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(54) **SEMICONDUCTOR HETEROSTRUCTURE DIODES**

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 H01L 33/00 (2006.01)
(52) **U.S. Cl.** **257/194**; 257/183; 257/199; 257/E29.195; 257/E33.03
(58) **Field of Classification Search** 257/183, 257/194, 199, E29.195, E33.03
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,914,489	A	*	4/1990	Awano 257/6
5,646,069	A		7/1997	Jelloian et al.
5,705,847	A	*	1/1998	Kashiwa et al. 257/476
7,084,475	B2		8/2006	Shelton et al.
2007/0132037	A1		6/2007	Hoshi et al.
2007/0145390	A1	*	6/2007	Kuraguchi 257/94
2007/0194354	A1		8/2007	Wu et al.
2009/0032879	A1	*	2/2009	Kuraguchi 257/368

FOREIGN PATENT DOCUMENTS

WO   2008/120094   10/2008

OTHER PUBLICATIONS

Wanjun Chen et al., "High-performance AlGaN/GaN lateral field-effect rectifiers compatible with high electron mobility transistors", Jun. 25, 2008, Applied Physics Letters, 92, 3 pp.
Mishra et al., "Enhancement Mode III-N HEMTs", U.S. Appl. No. 12/108,449, filed Apr. 23, 2008, 58 pp.
Rajan et al., "N-Polar Aluminum Gallium Nitride/Gallium Nitride Enhancement-Mode Field Effect Transistors", U.S. Appl. No. 11/523,286, filed Dec. 18, 2006, 25 pp.
Suh et al., "High Breakdown Enhancement Mode Gallium Nitride Based High Electron Mobility Tranistors With Integrated Slant Field Plate", U.S. Appl. No. 11/841,476, 25 pp.
Authorized officer Cheon Whan Cho, International Search Report and Written Opinion in PCT/US2009/066647, mailed Jul. 1, 2010, 16 pages.

* cited by examiner

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(57) **ABSTRACT**

Planar Schottky diodes for which the semiconductor material includes a heterojunction which induces a 2DEG in at least one of the semiconductor layers. A metal anode contact is on top of the upper semiconductor layer and forms a Schottky contact with that layer. A metal cathode contact is connected to the 2DEG, forming an ohmic contact with the layer containing the 2DEG.
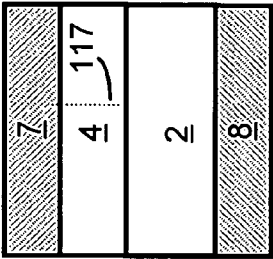
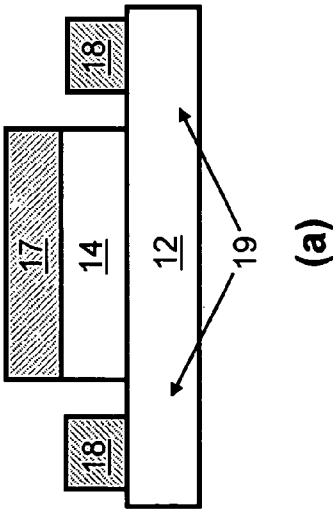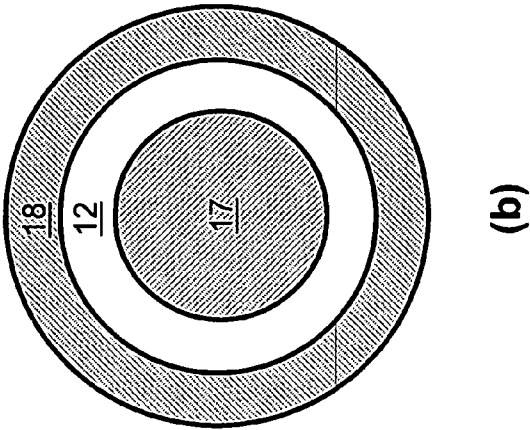**22 Claims, 19 Drawing Sheets**
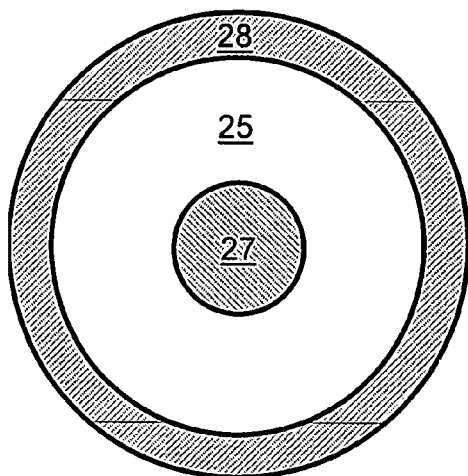
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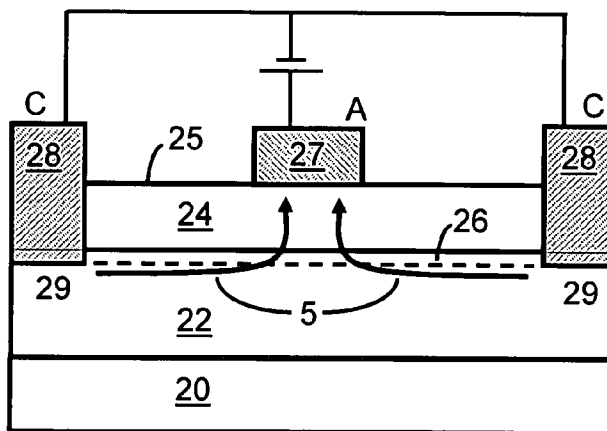
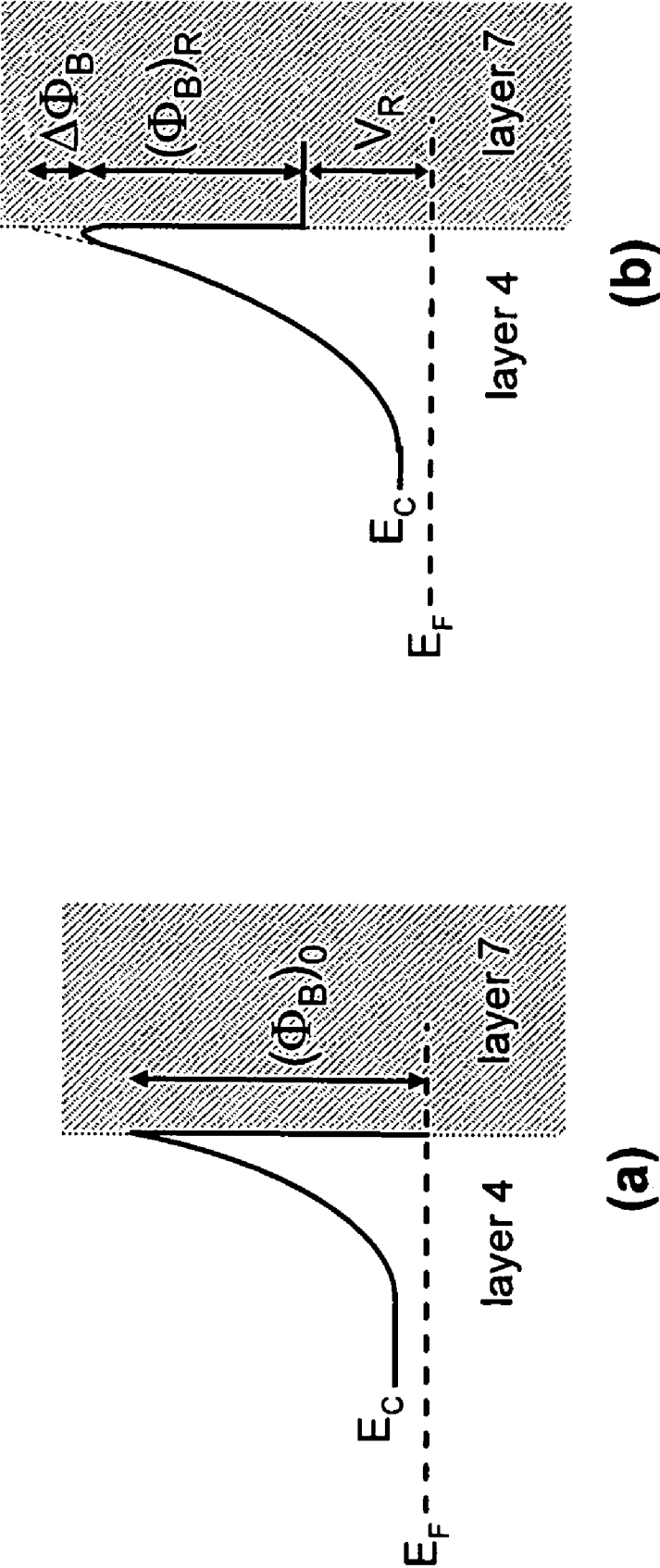

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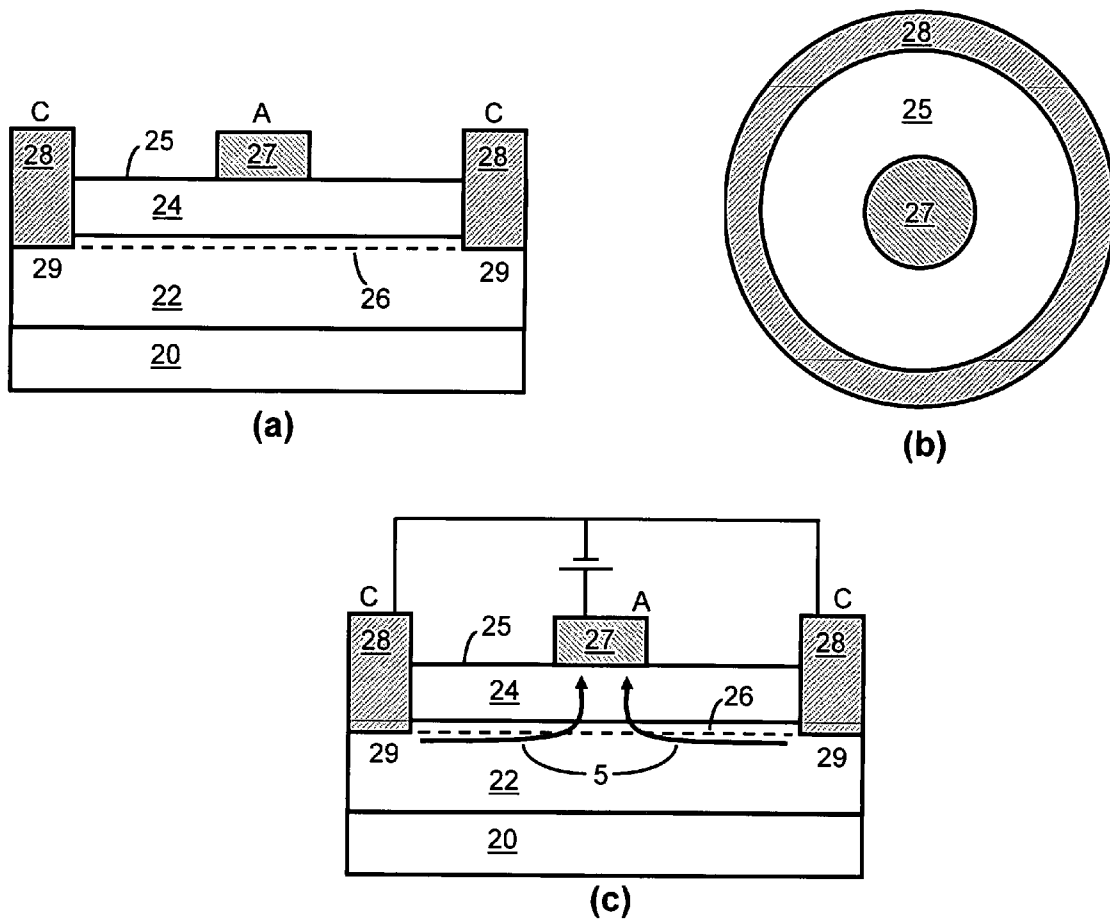
Figure 1
(prior art)

Figure 2
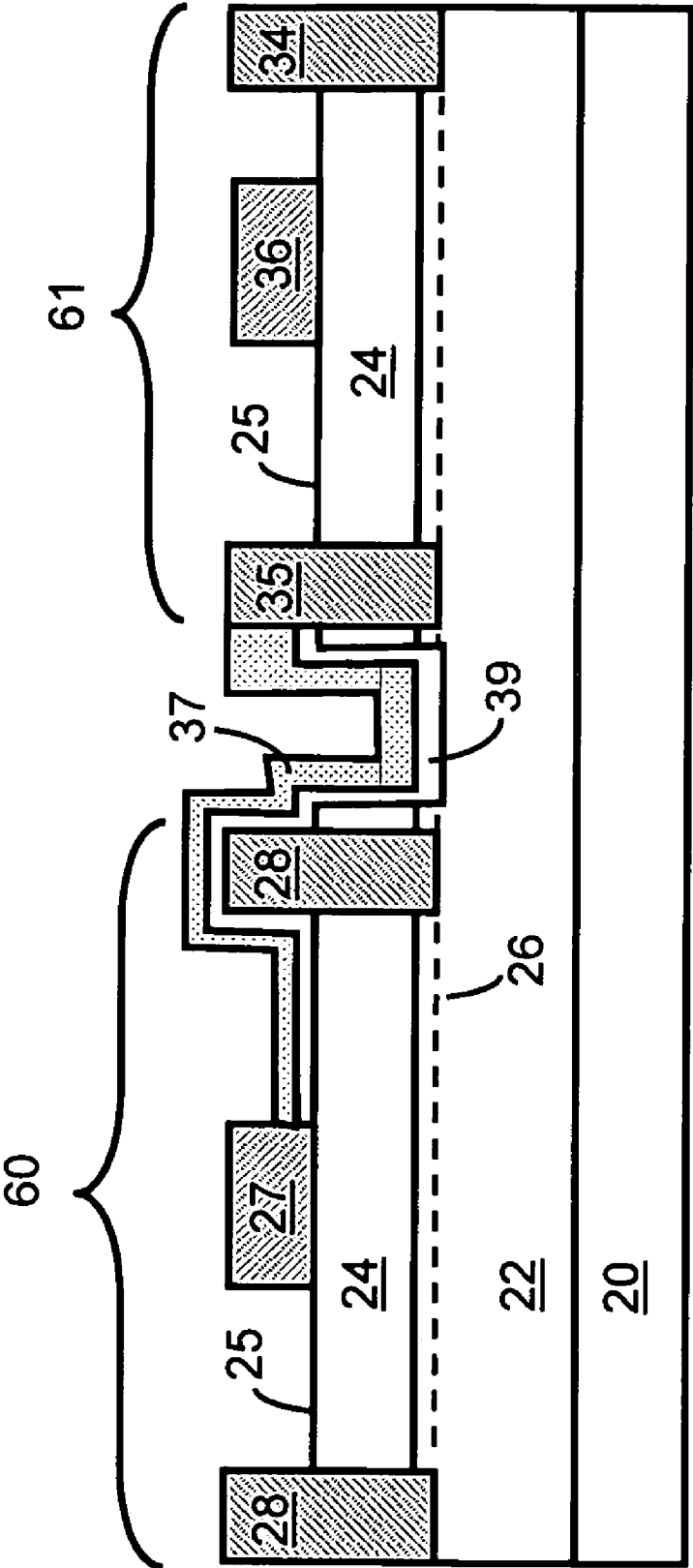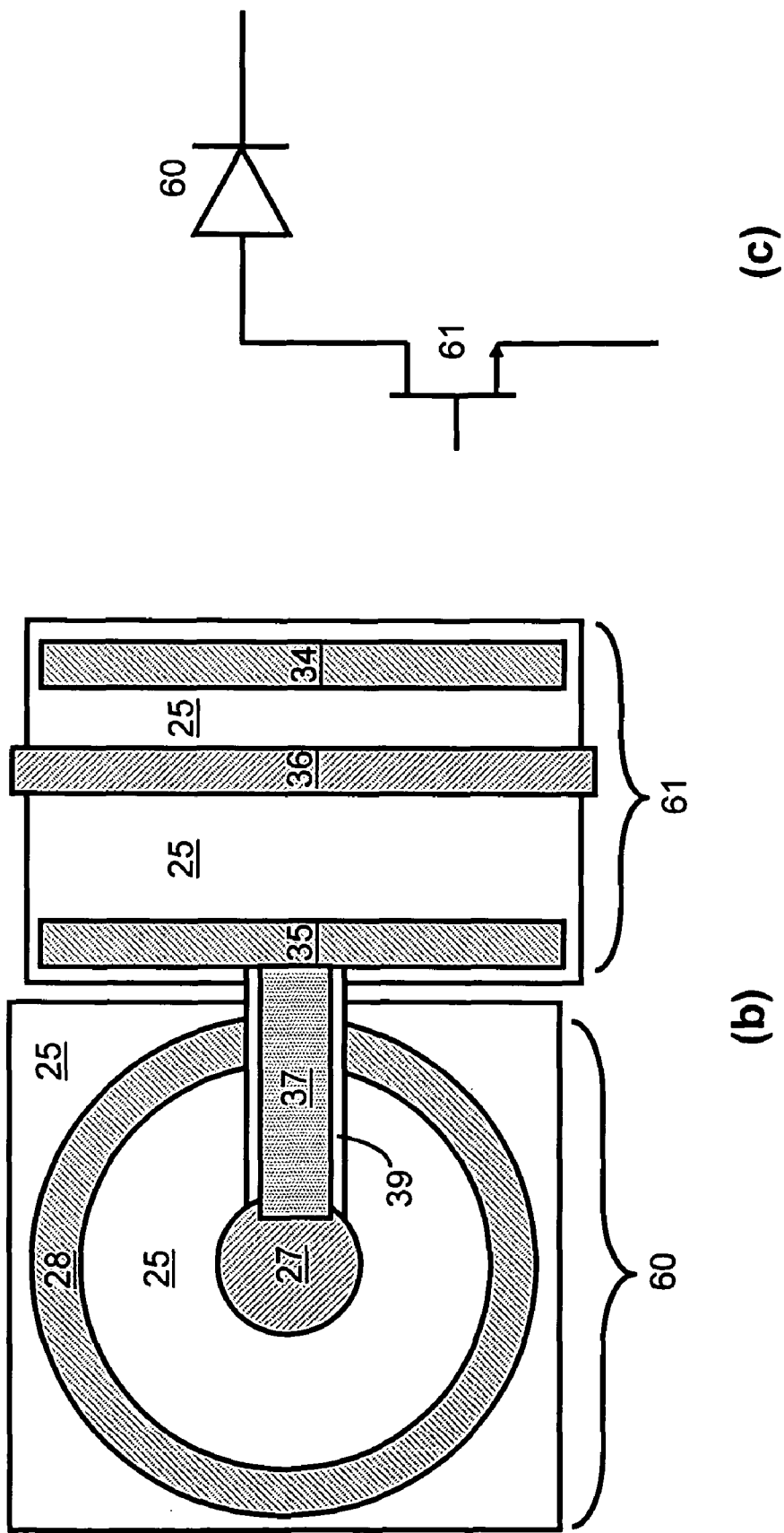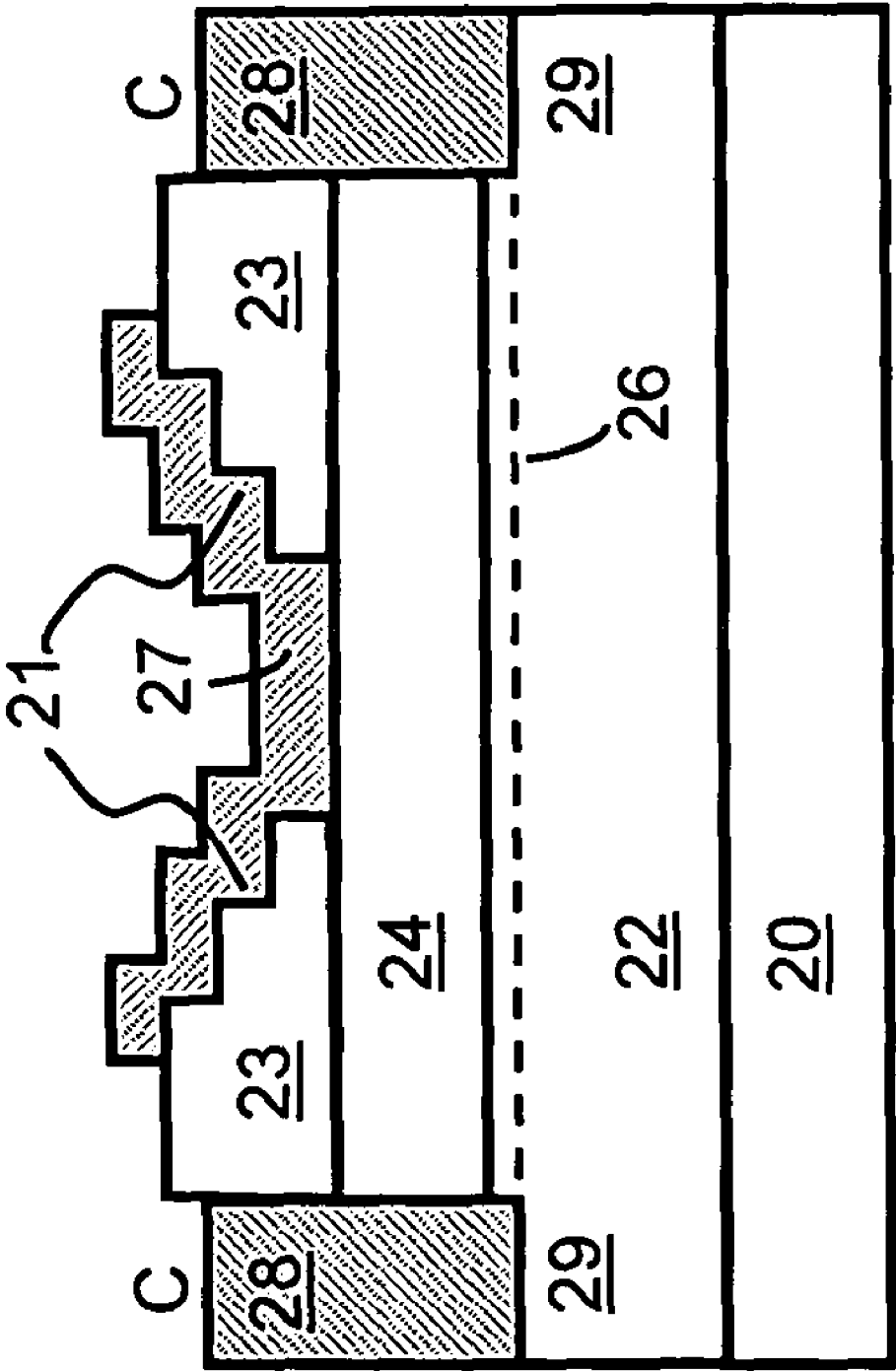(prior art)

(a)

(b)

Figure 3
(prior art)

(a)

(b)

(c)

Figure 4

(a)

Figure 5

Figure 5

Figure 6
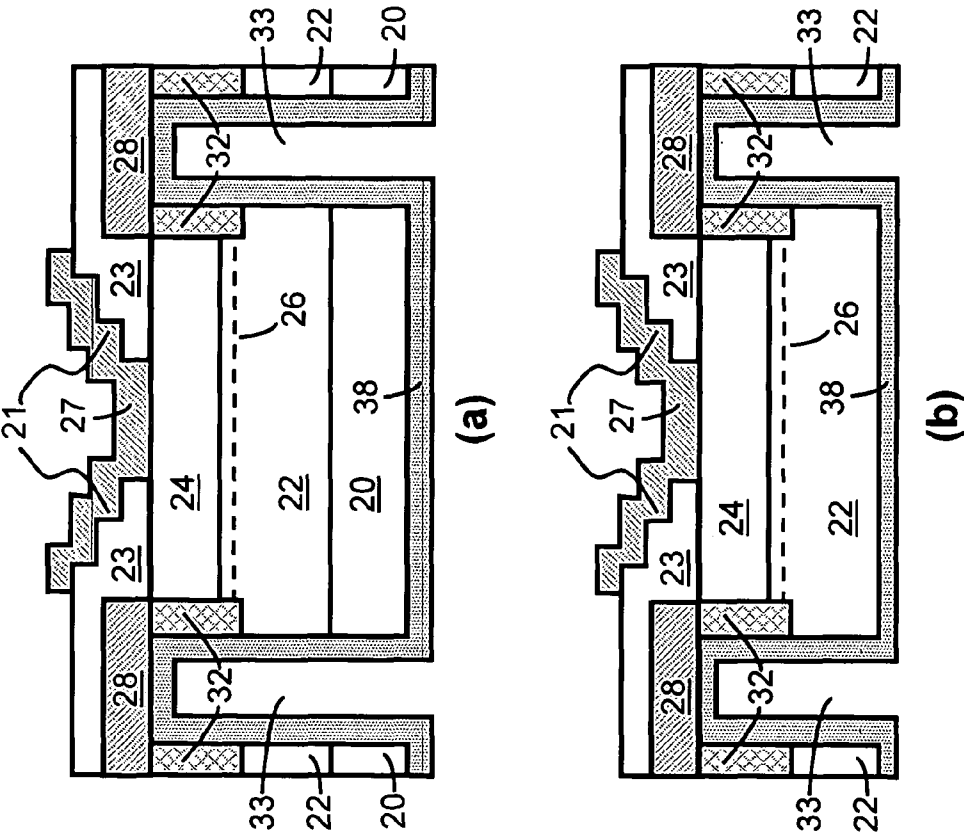
Figure 7

Figure 8

Figure 9

(a)

(b)
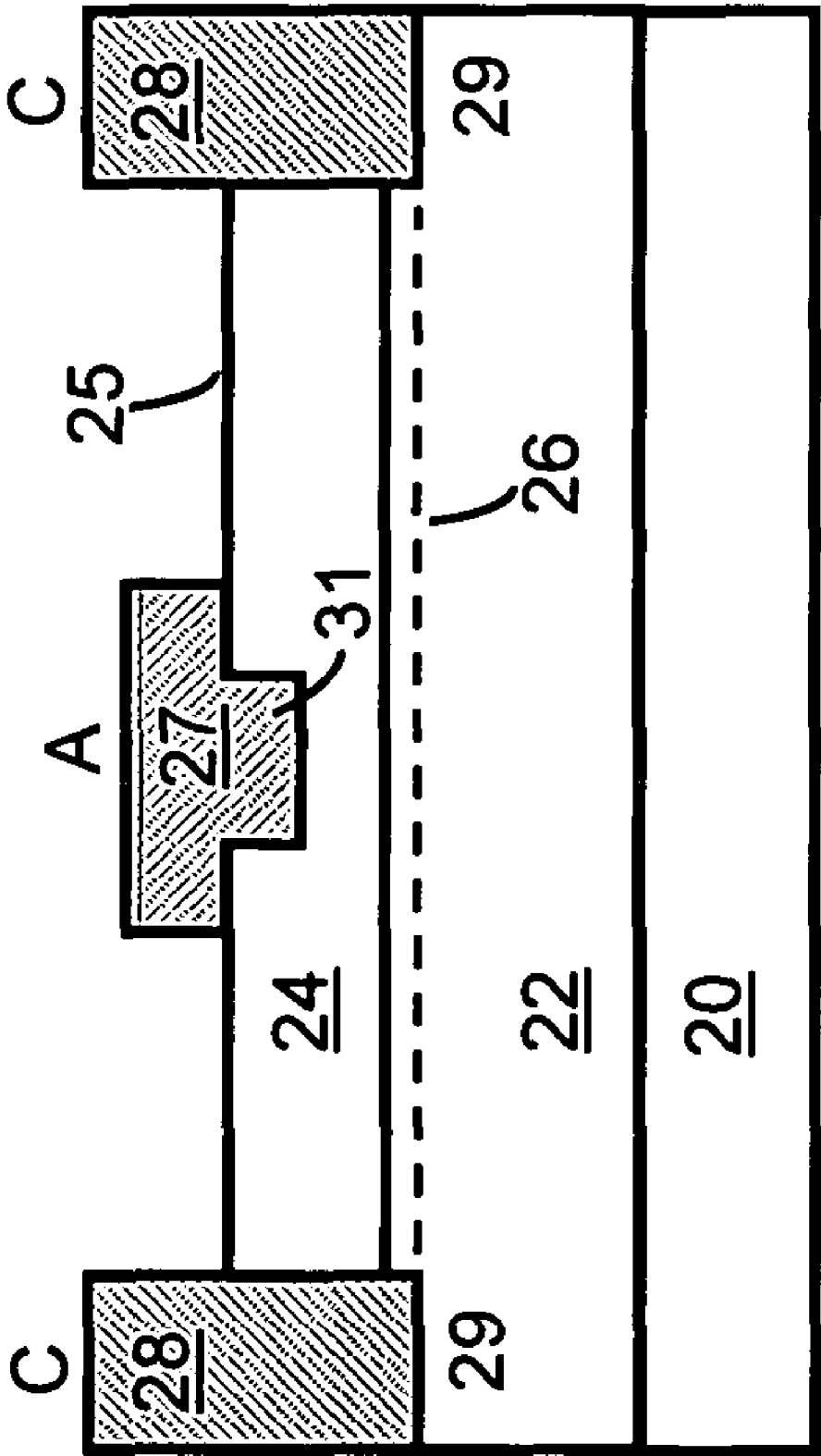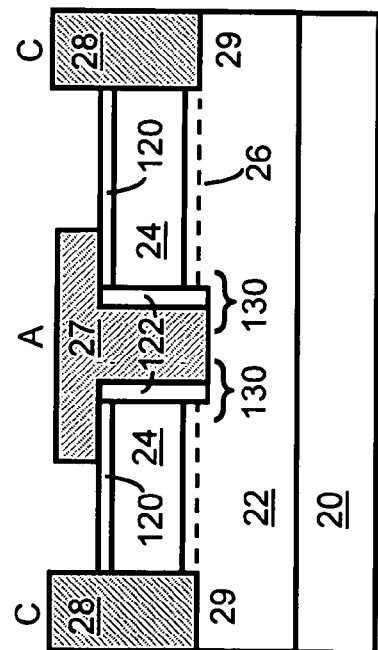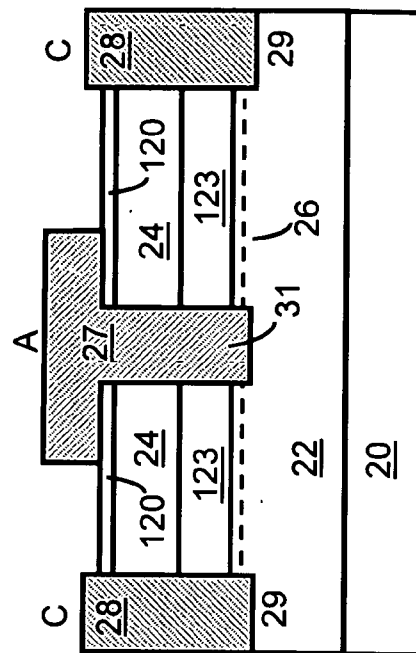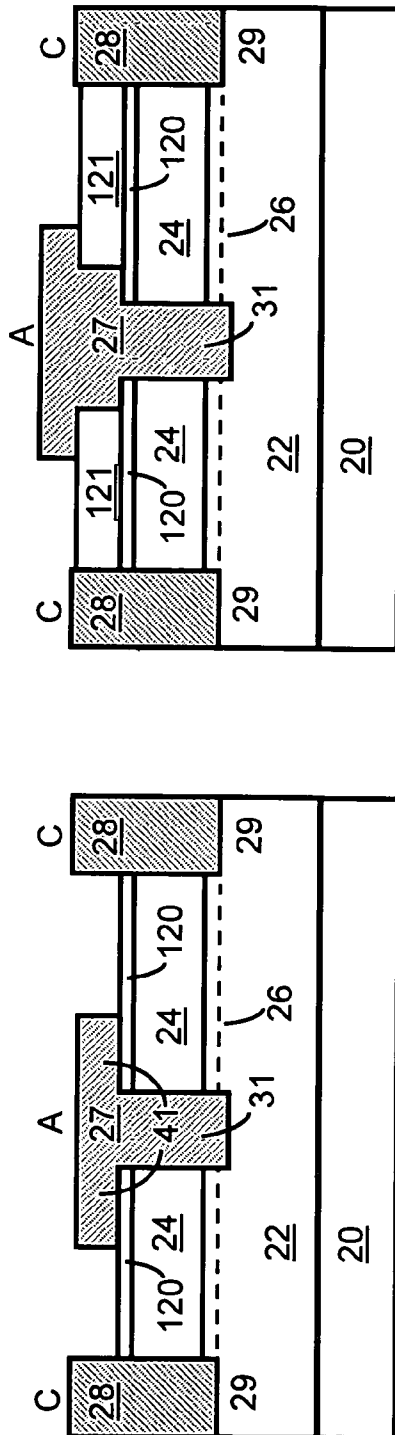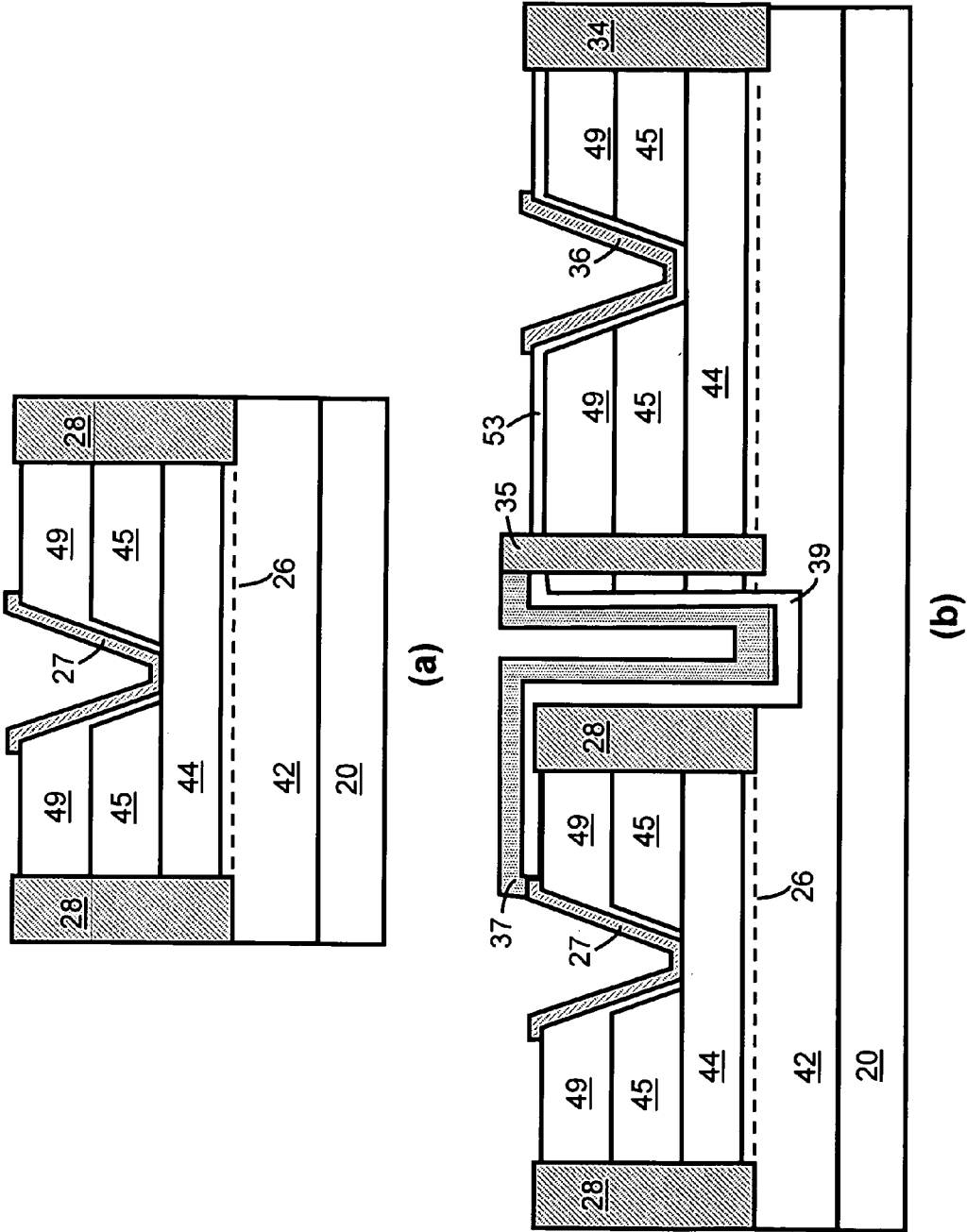
Figure 10

Figure 10

(a)

(b)
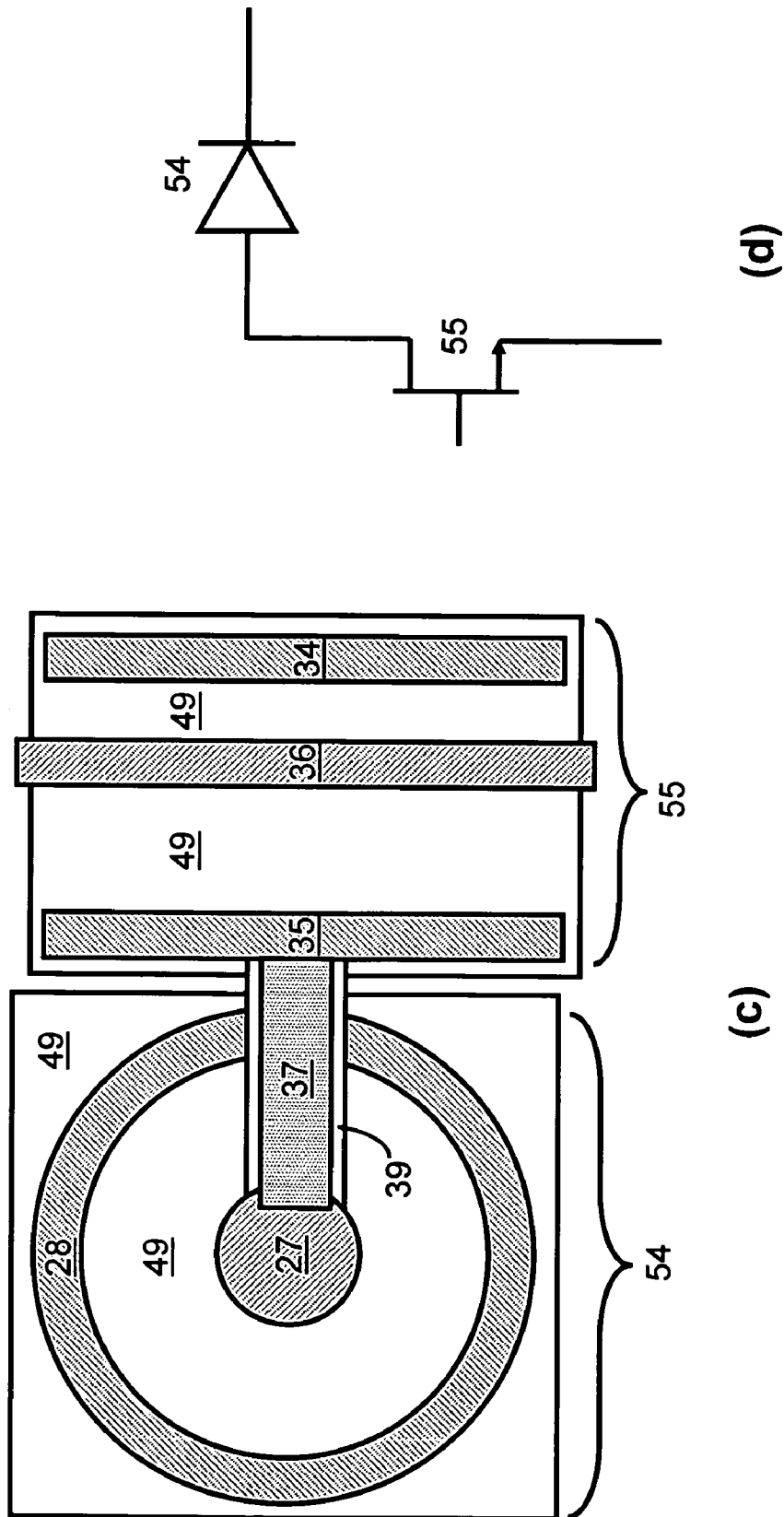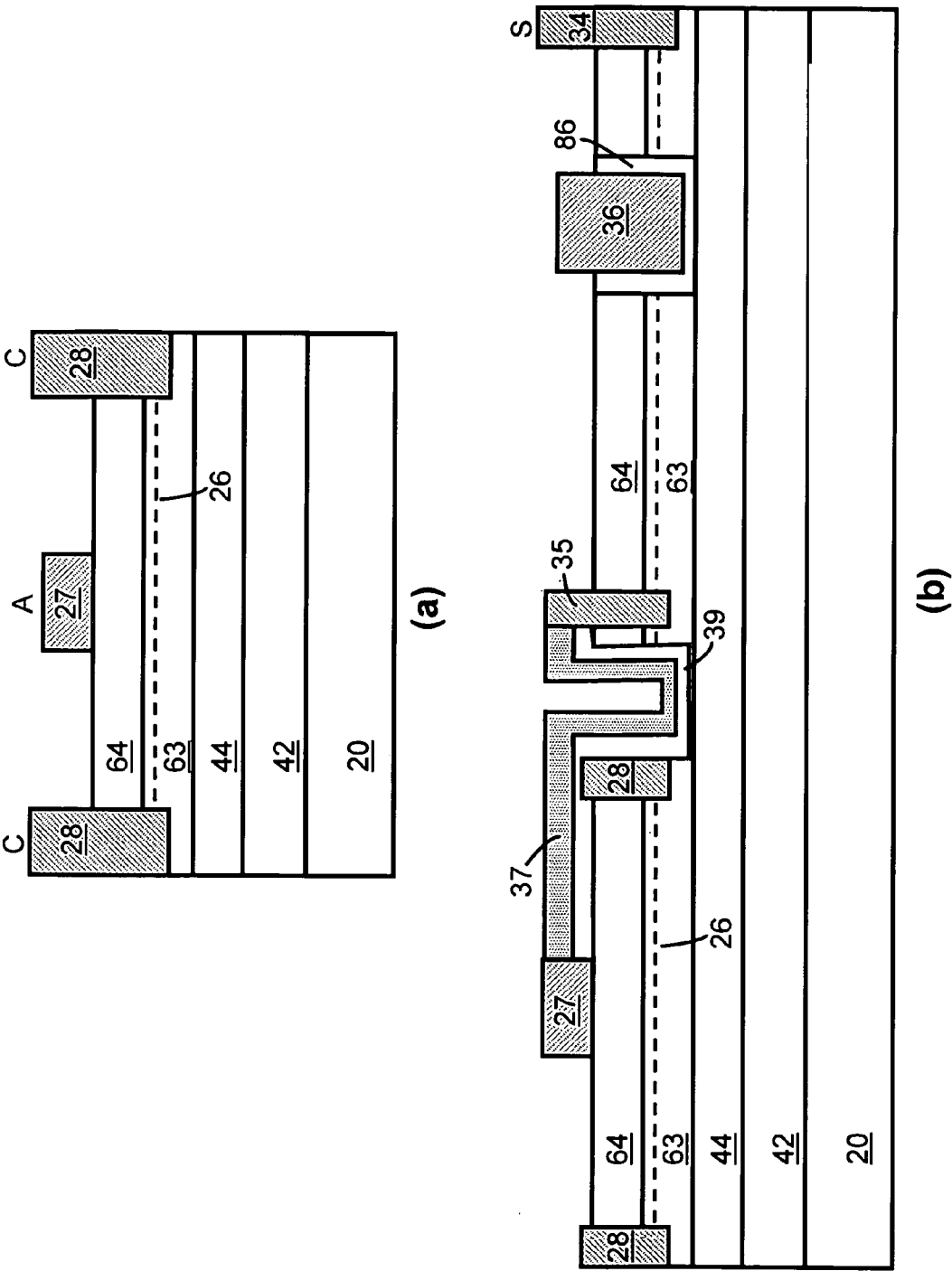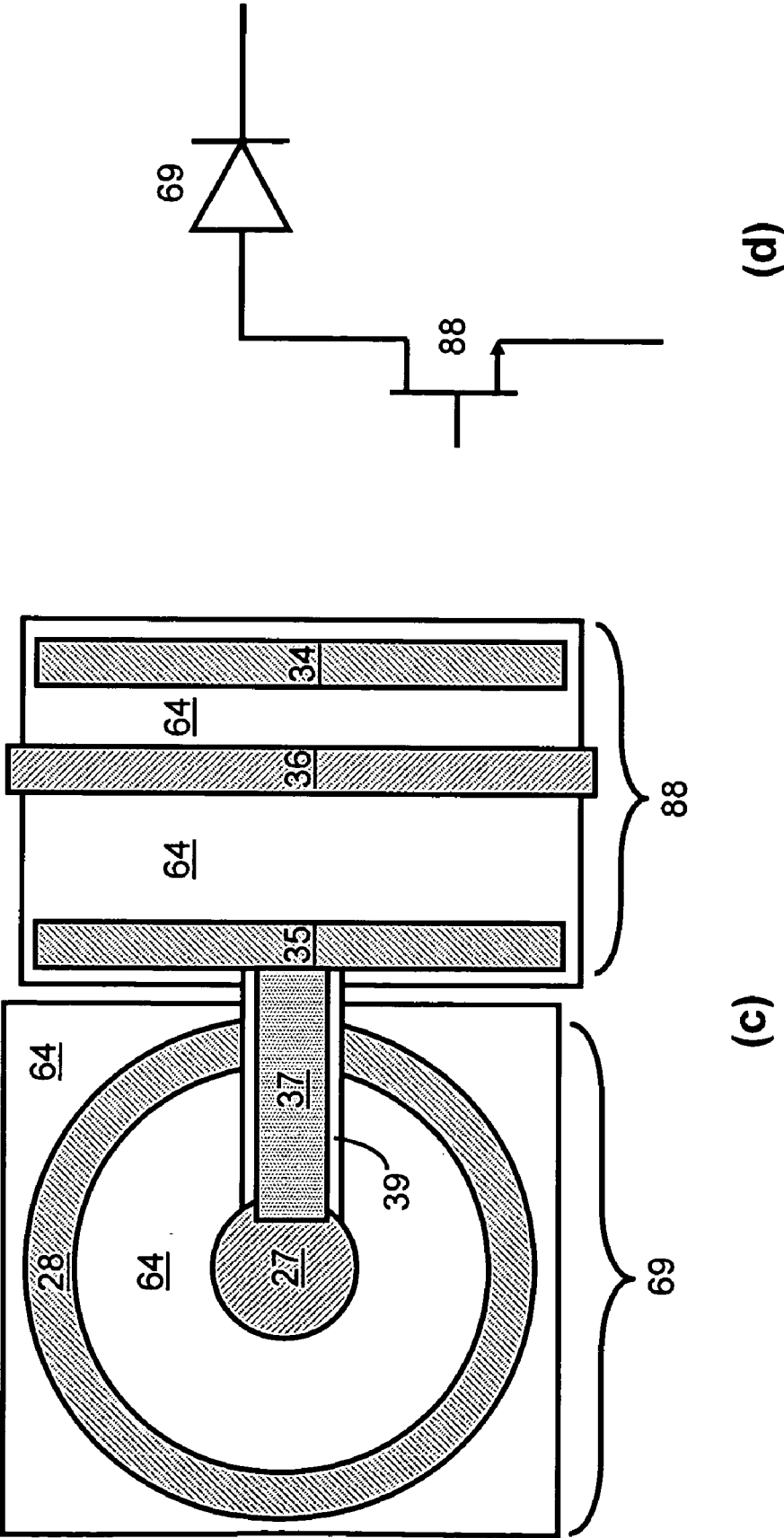
Figure 11

Figure 11
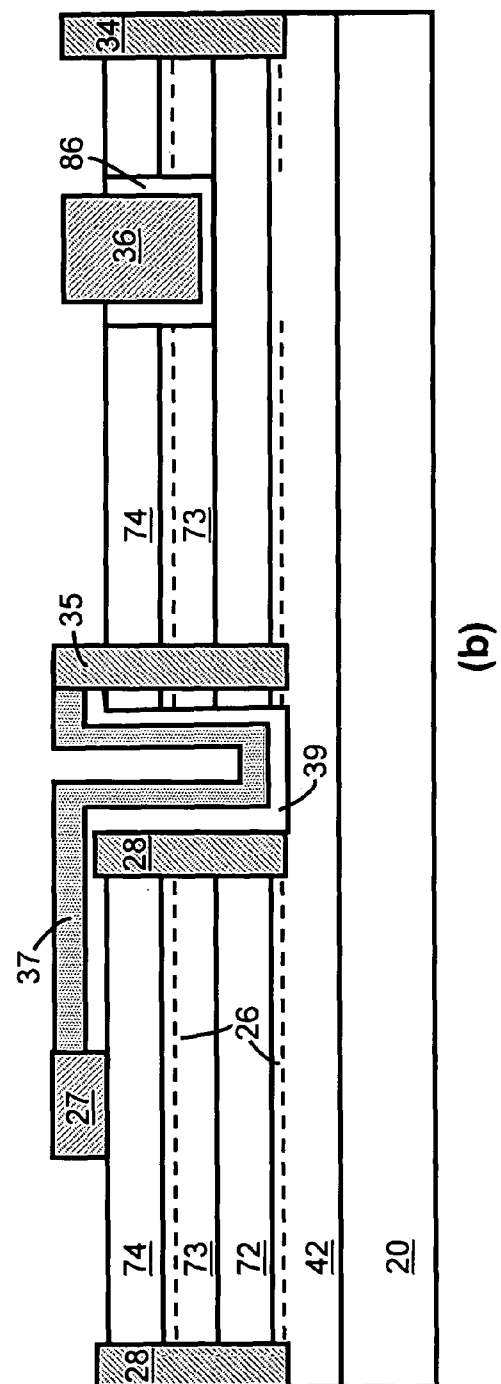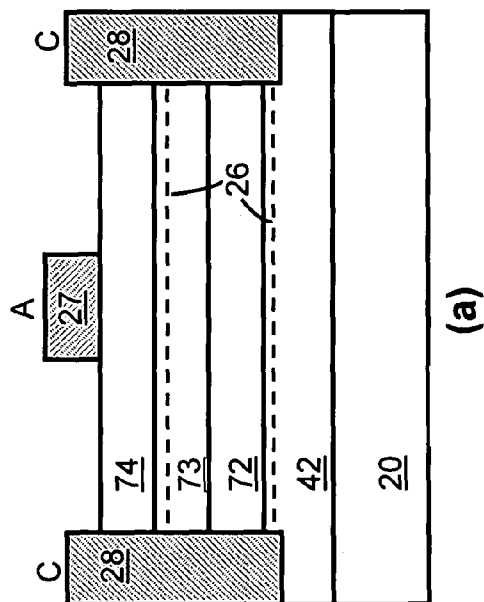
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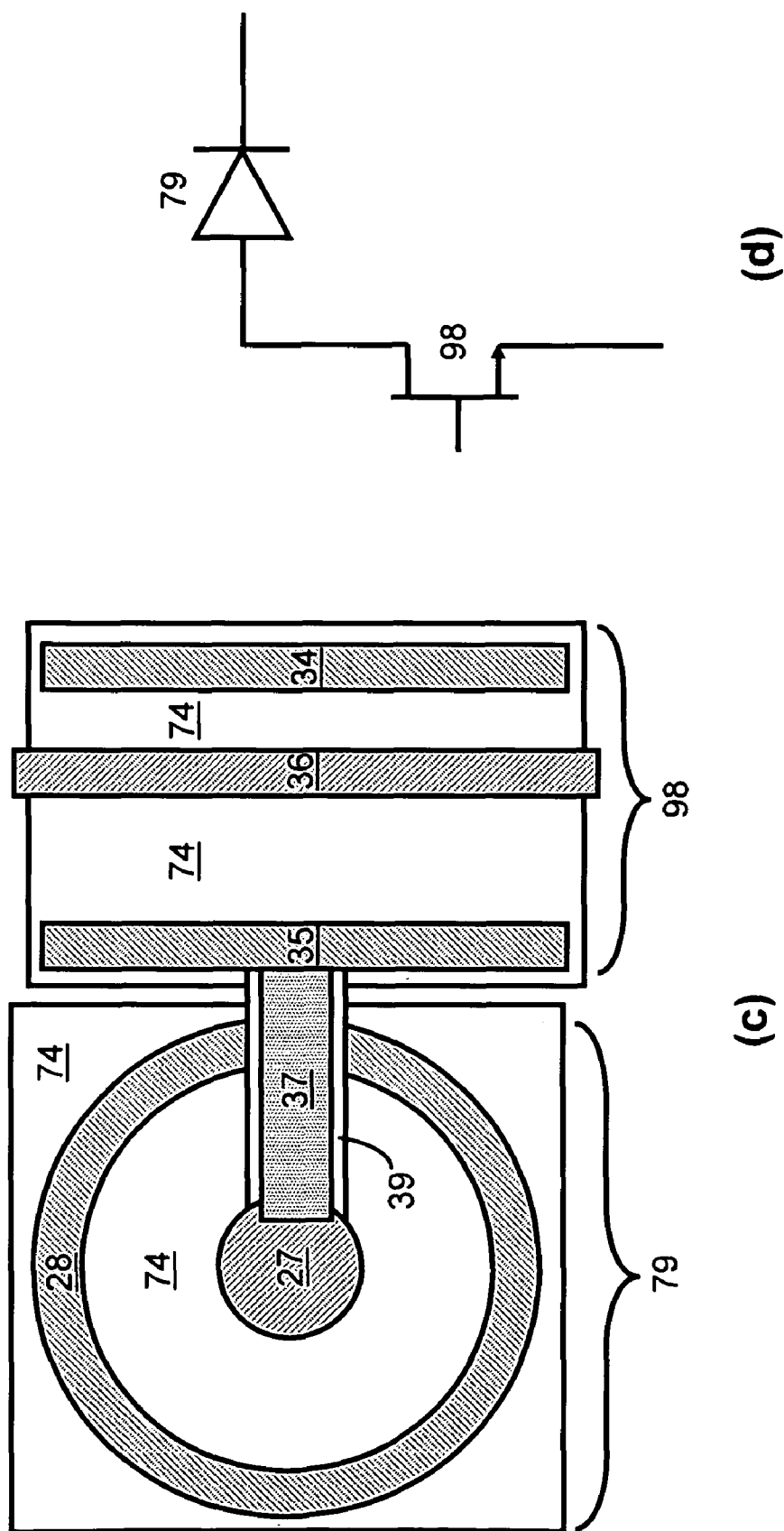
Figure 12

Figure 13

Figure 14

(a)

(b)
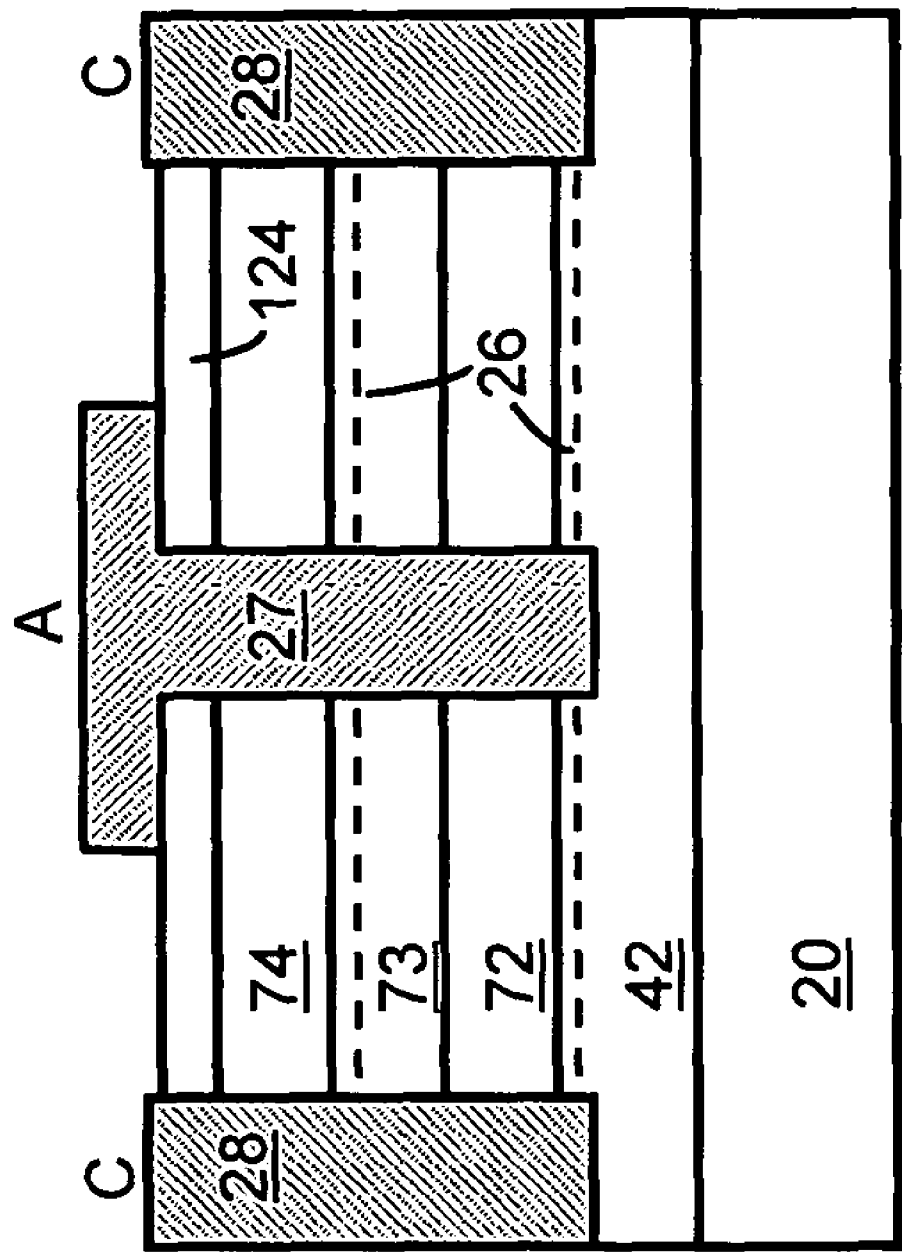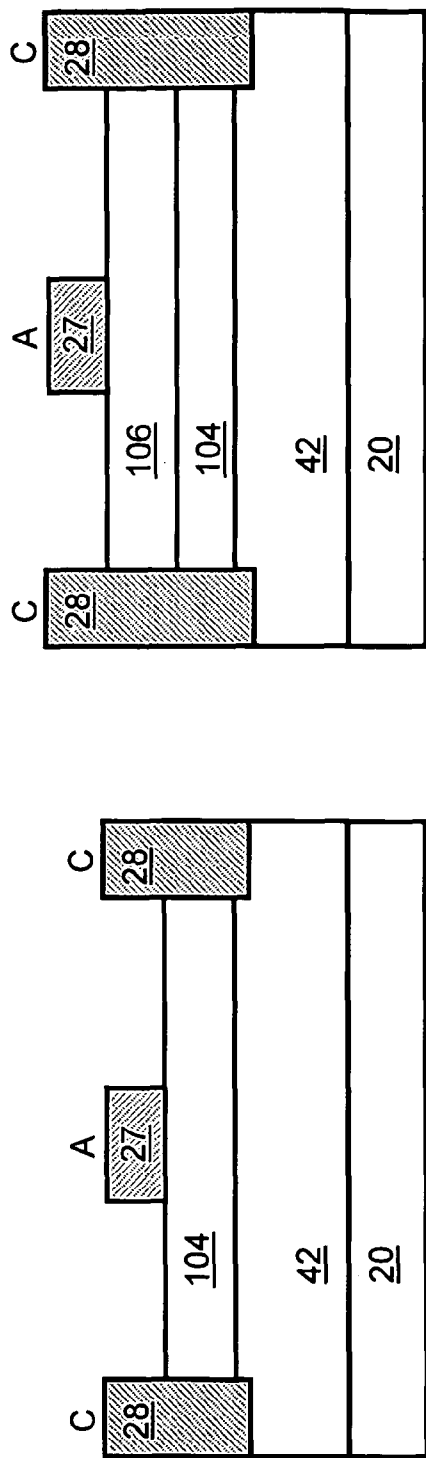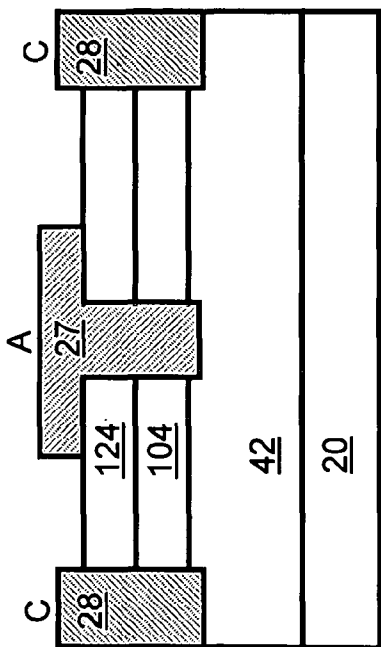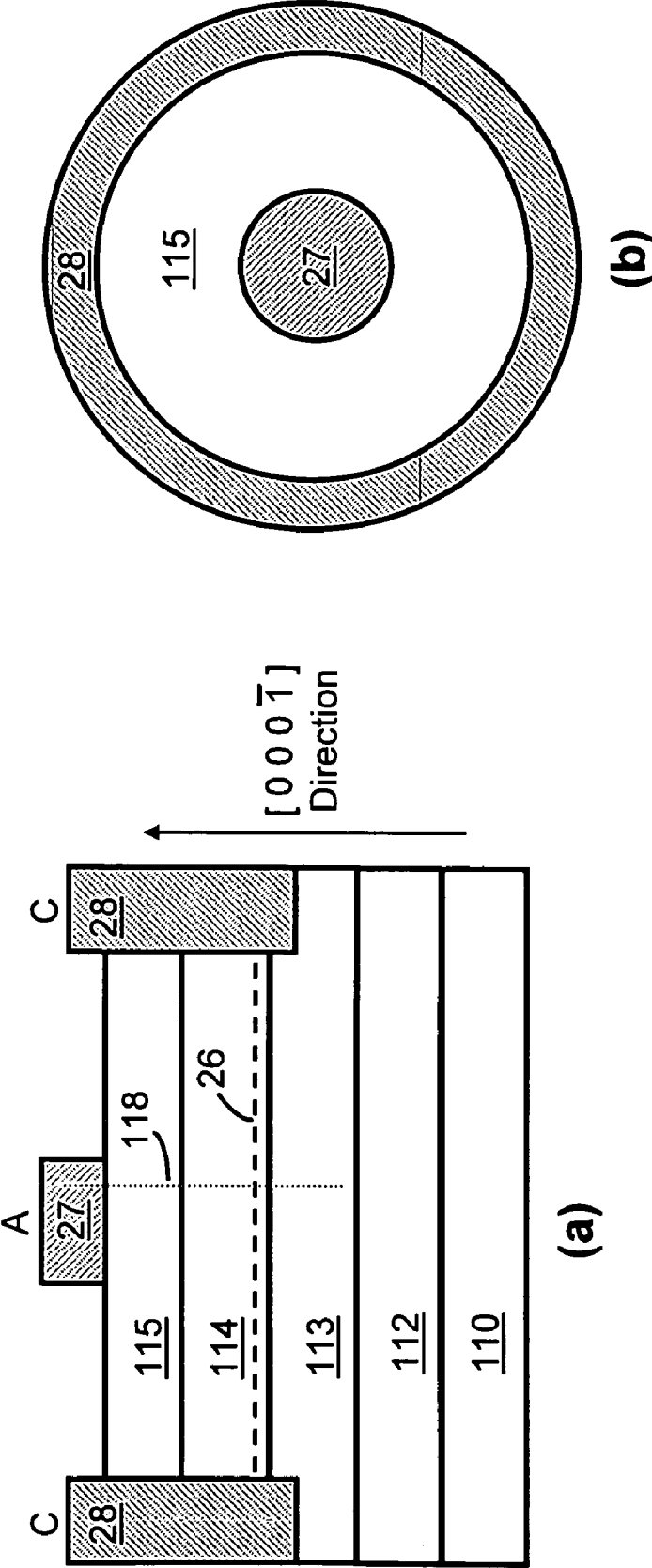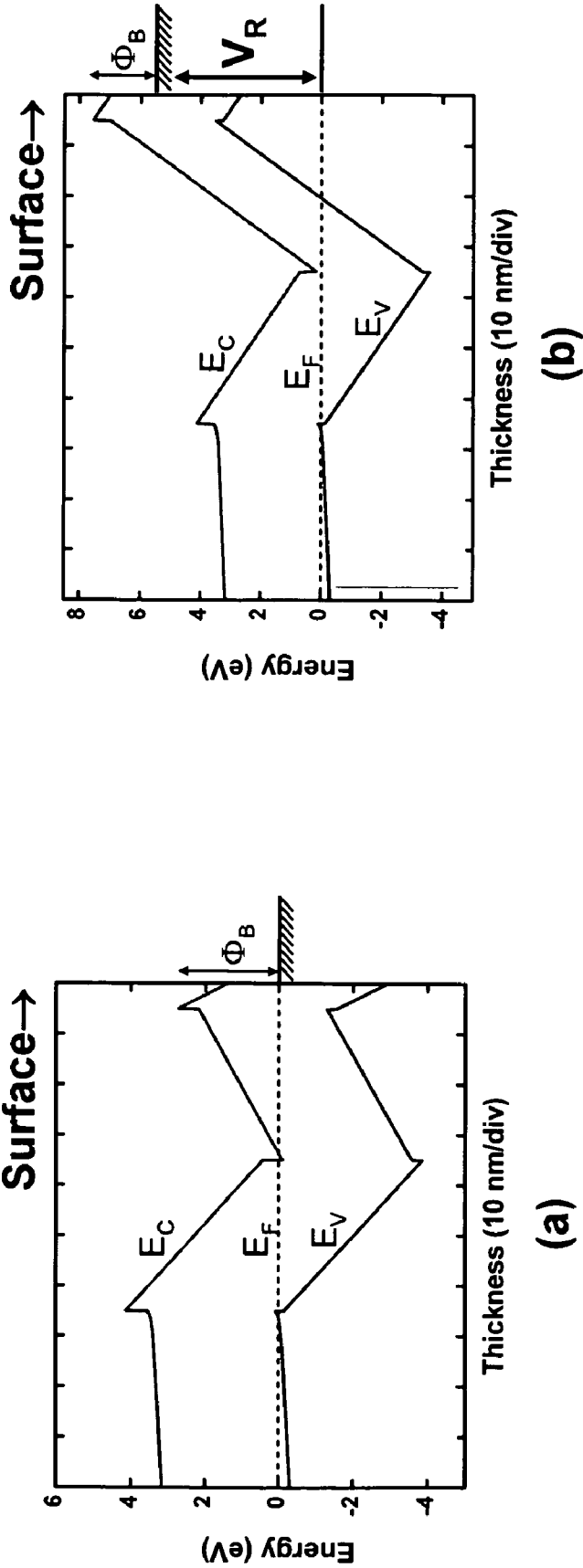
Figure 15

Figure 16

SEMICONDUCTOR HETEROSTRUCTURE DIODES

TECHNICAL FIELD

This invention relates to semiconductor electronic devices, specifically Schottky diodes based on semiconductor hetero-junctions.

BACKGROUND

Diodes are used in a wide range of electronic circuits. Diodes used in circuits for high voltage switching applications ideally require the following characteristics. When biased in the reverse direction (i.e., the cathode is at a higher voltage than the anode), the diode should be able to support a large voltage while allowing as little current as possible to pass through. The amount of voltage that must be supported depends on the application; for example, many high power switching applications require diodes that can support a reverse bias of at least 600V or at least 1200V without passing a substantial amount of current. When current flows through the diode in the forward direction (from anode to cathode), the forward voltage drop across the diode V_{on} should be as small as possible to minimize conduction losses, or in other words the diode on-resistance R_{on} should be as small as possible. Finally, the amount of charge stored in the diode when it is reverse biased should be as small as possible to reduce transient currents in the circuit when the voltage across the diode changes, thereby reducing switching losses.

In diodes, there is typically a trade-off between the various characteristics described above. For example, Silicon Schottky diodes can typically exhibit excellent switching speed and on-state performance but suffer from large reverse leakage currents, making them unsuitable for high voltage applications. Conversely, high voltage Si PIN diodes can support large reverse bias voltages with low leakage but typically exhibit high conduction and switching losses. Further, reverse recovery currents in PIN diodes add to transistor losses in circuits.

Illustrations of typical Schottky diodes are show in FIGS. 1 and 2. FIG. 1 shows a vertical diode structure. Layers 2 and 4 are comprised of a semiconductor material of the same conductivity type, wherein layer 2 is heavily doped and layer 4 is lightly doped. Metal layer 7 forms a Schottky anode contact to layer 4, and metal layer 8 forms an ohmic cathode contact to layer 2. Increasing the active device area and/or decreasing the thickness of semiconductor layer 4 reduces the forward operating voltage V_{on} but increases reverse-bias leakage.

FIGS. 2a and 2b show a lateral diode structure, wherein FIG. 2a is a cross-sectional view and FIG. 2b is a plan view (top view) of the diode structure. Layers 12 and 14 are comprised of a semiconductor material of the same conductivity type (i.e., they are either both n-type or both p-type), wherein layer 12 is heavily doped and layer 14 is lightly doped. Metal layer 17 forms a Schottky contact to layer 14, and metal layer 18 forms an ohmic contact to layer 2. This geometry can be preferable to a vertical one when a planar structure for the anode and cathode is required for packaging, or when the semiconductor material is epitaxially grown on an insulating substrate. The on-resistance R_{on} for the lateral geometry is typically larger than that for the vertical geometry due to the added lateral resistance of region 19 through which the forward current must travel. Additionally, as a result of the forward current flowing laterally outwards through a layer 12

with non-zero sheet resistance, the current through 14 tends to crowd towards the edges of the mesa, thereby further increasing the on-resistance.

In standard Schottky diodes, Schottky barrier lowering occurs when the diode is reverse biased, resulting in increased reverse bias currents. Schottky barrier lowering for the diode in FIG. 1 is illustrated schematically in the diagrams of FIGS. 3a and 3b. FIGS. 3a and 3b are band diagrams along dotted line 117 in FIG. 1, where FIG. 3a corresponds to zero applied bias, i.e. anode contact 7 and cathode contact 8 are at the same voltage, and FIG. 3b is for a reverse bias V_R, i.e. anode contact 7 is at a lower voltage than the cathode contact 8. The electric field in the structure is proportional to the slope of the conduction band EC in FIGS. 3a and 3b. The Schottky barrier height in FIG. 3b, $(\Phi_B)_R$, is less than that in FIG. 3a, $(\Phi_B)_0$, by an amount $\Delta\Phi_B$, where $\Delta\Phi_B$ increases as the maximum electric field near the metal-semiconductor junction increases, which occurs when V_R is increased. This lowering of the Schottky barrier results in increased reverse bias currents as the reverse voltage across the device is increased.

It is desirable to provide diodes for which high blocking voltages can be achieved while at the same time maintaining lower on-resistances. Diode structures which can easily be integrated with other circuit components, such as transistors, are desirable for process integration and cost reduction. Additionally, Schottky diodes for which Schottky barrier lowering is mitigated are desirable, since lower reverse leakage currents can potentially be achieved.

SUMMARY

Semiconductor Schottky diodes with low on-resistance, high breakdown voltage, and low reverse leakage currents are described. Devices described herein include a two-dimensional electron gas (2DEG) to reduce on-resistance and conduction losses and can include one or more of the following features. A diode can include a field plate or multiple field plates to increase the breakdown voltage. A diode can include a Schottky barrier which is not lowered during reverse bias operation. A diode can be integrated with a semiconductor transistor on the same substrate.

In one aspect, a diode is described. The diode includes a first III-N material layer, a second III-N material layer and two terminals. The second III-N material layer is on the first III-N material layer, wherein a 2DEG channel is in the first III-N material layer because of a compositional difference between the first III-N material layer and the second III-N material layer. A first terminal is an anode consisting of a Schottky contact formed with the second III-N material layer and a second terminal is a single cathode in ohmic contact with the 2DEG channel.

In another aspect, a diode is described. The diode includes a first III-N material layer, a second III-N material layer, a third III-N material layer, a fourth III-N material layer and two terminals. The second III-N material layer is on the first III-N material layer. The second III-N material layer differs in composition from the first III-N layer. The third III-N material layer is on the second III-N material layer and differs in composition from the second III-N material layer. The fourth III-N material layer is on the third III-N material layer. A 2DEG channel is induced in the third III-N material layer adjacent to the fourth III-N material layer because of a compositional difference between the third III-N material layer and the fourth III-N material layer. A first terminal is an anode consisting of a Schottky contact with the fourth III-N material layer and a second terminal is a single cathode in ohmic contact with the 2DEG channel.

In yet another aspect, a diode is described that includes a first III-N material layer, a second III-N material layer, an anode and a single cathode. The second III-N material layer is compositionally graded and has a channel consisting of a polarization-induced charge distribution. The anode consists of a Schottky contact with the second III-N material layer. The cathode is in ohmic contact with the channel.

In another aspect, a diode is described that includes a substrate, a first III-N material layer on the substrate, a second III-N material layer on the first III-N material layer, wherein the second III-N material layer is compositionally different from the first III-N material layer, a third III-N material layer on the second III-N material layer and two terminals. A 2DEG channel is in the second III-V material layer adjacent to the first III-V material layer because of a compositional difference between the first III-N material layer and the second III-N material layer and the first, second, and third III-N material layers are N-polar or nitrogen-terminated semi-polar material. One terminal is an anode consisting of a Schottky contact with an N-face of the third III-N material layer and one terminal is a single cathode in ohmic contact with the 2DEG channel.

In yet another aspect, a diode is described that includes a first III-N material layer, a second III-N material layer on the first III-N material layer, a first insulator layer on the first III-N material layer so that the second III-N material layer is between the first insulator layer and the first III-N material layer and two terminals. The second III-N material layer has a thickness and a first 2DEG channel is in the first III-N material layer because of a compositional difference between the first III-N material layer and the second III-N material layer. The insulator layer is less than 7 nm thick. The first terminal is an anode that extends through an entirety of the thickness of the second III-N material layer to contact the first III-N material layer and form a Schottky contact with the first III-N material layer and has extending portions that extend over the first insulator layer and a second terminal is a single cathode in ohmic contact with the first 2DEG channel.

In another aspect a diode is described that includes a first III-N material layer, a second III-N material layer on the first III-N material layer, a third III-N material layer, a fourth III-N material layer and two terminals. The second III-N material layer has a thickness and a first 2DEG channel is in the first III-N material layer because of a compositional difference between the first III-N material layer and the second III-N material layer. The second III-N material layer is between the first III-N material layer and the third III-N material layer. The third III-N material layer is between the fourth III-N material layer and the second III-N material layer and a second 2DEG is in the third III-N material layer because of a compositional difference between the third III-N material layer and the fourth III-N material layer. A first terminal is an anode that extends through an entirety of the thickness of the second III-N material layer to contact the first III-N material layer and form a Schottky contact with the first III-N material layer and has extending portions that extend over the first insulator layer and a second terminal is a single cathode in ohmic contact with the first 2DEG channel.

In another aspect, a diode is described that includes a first III-N material layer, a second III-N material layer, wherein the second III-N material layer has a thickness and is compositionally graded and has a channel consisting of a polar-ization-induced charge distribution, an anode forming a Schottky contact with the second III-N material layer, wherein the anode extends through an entirety of the thickness of the second III-N material layer and has extending

portions that extend over the second III-N material layer and a single cathode in ohmic contact with the channel.

In yet another aspect, a diode is described that includes a III-N semiconductor material, an anode Schottky contact, and a cathode contact, wherein a Schottky barrier height of the anode contact is not substantially reduced when the diode is reverse biased as compared to when the anode and cathode contacts are at the same voltage.

Embodiments may include one or more of the following features. When the diode is forward biased, current can flow from the anode to the cathode predominantly through a Schottky barrier and the 2DEG channel. The first III-N material layer can include GaN. The second III-N material layer can be recessed in a location corresponding to the anode. A field plate can be electrically connected to the anode. An insulating layer can surround the anode and be between the field plate and the second III-N material layer. The second III-N material layer can include a recess in which a backside electrically conductive layer electrically contacts the cathode. A region of the second III-N material layer can be n-type, the region contacting the cathode and the conductive layer. A third III-N material layer can be on a side of the second III-N material layer opposite to the first III-N material layer and an insulator layer can be on the third III-N material layer opposite to the second III-N material layer, wherein the third III-N material layer is at least five times thicker than the second III-N material layer and is doped, and the anode is in a recess in the third III-N material layer and the insulator layer. A second 2DEG channel can be induced in the first III-N material layer adjacent to the second III-N material layer. Grading in a layer can induce n-type conductivity. An entirety of the second III-N material layer can be graded. The first III-N material layer and second III-nitride material layer can be oriented in a polar direction. The layers can be oriented in a [0 0 0 1] polar direction. The first III-N material layer and the second III-N material layer can be oriented in a semi-polar direction. The semi-polar direction can be a gallium termi-nated semi-polar direction. The second III-N material layer can be $Al_xGa_{1-x}N$, where x changes from about 0 to less than 0.3 from a portion of the layer adjacent to the first III-N material layer to a portion adjacent to the third III-N material layer and the third III-N material layer can either be GaN or $Al_zGa_{1-z}N$. z can be larger than the maximum value of x and a 2DEG is in the second III-N material layer. z can be less than the maximum value of x. The first III-N material layer can be doped. With some diodes, the Schottky barrier height is not substantially reduced when the diode is reverse biased. A field plate can extend from the extending portions of the anode and the second insulator layer is between the field plate and the first insulator layer. Sidewall insulating material can surround a lateral sidewall of the anode, wherein a horizontal portion of the anode contacts the first III-N material layer. One of the III-N material layer can be AlN. An insulator can be between the extending portions and the fourth III-N material layer and a sidewall insulator can be between a lateral side of the anode and the second III-N material layer, wherein a bottom side of the anode makes the Schottky contact with the first III-N material layer. An insulator layer can be on the second III-N material layer, wherein the insulator layer is between the second III-N material layer and the extending portions of the anode.

An assembly can be formed from any of the diode described herein. An assembly can also include a III-N tran-sistor, where a terminal of the two terminals of the diode is electrically connected to a terminal of a III-N transistor. The anode of the diode can be electrically connected to a drain of the III-N transistor. The diode and the III-N transistor can be

on a common substrate. An assembly can include an enhancement mode III-N transistor, wherein a terminal of the diode is electrically connected to a terminal of the III-N transistor.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a cross-sectional view of a diode device of the prior art.

FIGS. 2a and 2b are cross-sectional and plan views, respectively, of a diode device of the prior art.

FIGS. 3a and 3b are band diagrams of the device in FIG. 1 during various operating conditions.

FIGS. 4a and 4b are cross-sectional and plan views, respectively, of one embodiment of a semiconductor diode.

FIG. 4c shows the path of electron flow through the device of FIG. 4a during one mode of operation.

FIGS. 5a and 5b are cross-section and plan views, respectively, of the device in FIG. 4 integrated in series with a HEMT device.

FIG. 5c is a circuit schematic for the layout in FIGS. 5a and 5b.

FIG. 6 is a cross-sectional view of an embodiment of a semiconductor diode.

FIGS. 7a and 7b are cross-sectional views of other embodiments of semiconductor diodes.

FIG. 8 is a cross-sectional view of an embodiment of a semiconductor diode.

FIGS. 9a, 9b, 9c, and 9d are cross-sectional views of other embodiments of semiconductor diodes.

FIG. 10a is a cross-sectional view of an embodiment of a semiconductor diode.

FIGS. 10b and 10c are cross-section and plan views, respectively, of the device in FIG. 10a integrated in series with a HEMT device.

FIG. 10d is a circuit schematic for the layout in FIGS. 10b and 10c.

FIG. 11a is a cross-sectional view of an embodiment of a semiconductor diode.

FIGS. 11b and 11c are cross-sectional and plan views, respectively, of the device in FIG. 11a integrated in series with a HEMT device.

FIG. 11d is a circuit schematic for the layout in FIGS. 11b and 11c.

FIG. 12a is a cross-sectional view of an embodiment of a semiconductor diode.

FIGS. 12b and 12c are cross-sectional and plan views, respectively, of the device in FIG. 12a integrated in series with a HEMT device.

FIG. 12d is a circuit schematic for the layout in FIGS. 12b and 12c.

FIG. 13 is a cross-sectional view of an embodiment of a semiconductor diode.

FIGS. 14a, 14b, and 14c are cross-sectional views of embodiments of semiconductor diodes.

FIGS. 15a and 15b are cross-sectional and plan views, respectively, of an embodiment of a semiconductor diode.

FIGS. 16a and 16b are band diagrams of the device in FIG. 15a during various operating conditions.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Diodes based on semiconductor heterostructures that can support high reverse-bias voltages while at the same time exhibit low on-resistance R_{on} as well as low switching losses are described. An embodiment of this invention is shown in FIGS. 4a and 4b, wherein FIG. 4a is a cross-sectional view and FIG. 4b is a plan view (top view) of this embodiment. Briefly, the semiconductor device of this embodiment includes a substrate 20, a first semiconductor layer 22 on top of the substrate, and a second semiconductor layer 24 on top of the first semiconductor layer. Semiconductor layers 22 and 24 have different compositions from one another, the compositions selected such that a two-dimensional electron gas (2DEG) 26 is induced in the first semiconductor layer 22 near the interface between the first and second semiconductor layers 22 and 24. An anode contact 27 or a plurality of contacts are formed on top of surface 25 of the second semiconductor layer 24, and a single cathode contact 28 is formed which contacts the 2DEG 26 and is in close proximity to at least a portion of anode contacts 27. As used herein, the term "single cathode contact" refers to either a single metallic contact which serves as a cathode, or to a plurality of contacts serving as cathodes which are electrically connected such that the electric potential at each contact is about the same. As used herein, two or more contacts or other items are said to be "electrically connected" if they are connected by a material which is sufficiently conducting to ensure that the electric potential at each of the contacts or other items is about the same at all times. Anode and cathode contacts 27 and 28 may be any arbitrary shape, although the shape is ideally optimized to minimize the device area required for a given forward current. The anode contact 27 is a Schottky contact, and the single cathode contact 28 is an ohmic contact.

As stated earlier, semiconductor layers 22 and 24 have different compositions from one another. The compositions are selected such that the second semiconductor layer 24 has a larger bandgap than the first semiconductor layer 22, which helps enable the formation of 2DEG 26. The polarization fields, including both spontaneous and piezoelectric polarization, in semiconductor layers 22 and 24 can be different from one another and can contribute to inducing the 2DEG 26. If semiconductor layers 22 and 24 are composed of non-polar semiconducting material, then doping all or part of the second semiconductor layer 24 with an n-type impurity may also be required to induce the 2DEG. If at least one of semiconductor layers 22 and 24 is composed of a polar semiconducting material, and the polarization field in at least one of these layers has a component in a direction normal to surface 25, then 2DEG 26 may be induced by the polarization fields without the need for any substantial doping of either of the semiconductor layers, although the 2DEG sheet charge concentration can be increased by doping all or part of the second semiconductor layer 24 with an n-type impurity.

III-V semiconductor materials can be used for layers 22 and 24, wherein the compositions of the III-V layers are chosen such that the requirements for layers 22 and 24 are satisfied. High-electron mobility transistor (HEMT) devices can utilize a similar set of semiconductor materials to induce a 2DEG channel in said devices. As an example, semiconductor layer 22 can be GaN and layer 24 AlGaN, wherein layer 24 can be n-doped or can contain no significant concentration of doping impurities. In the case that layer 24 is undoped, the induced 2DEG results from the difference in polarization

fields between layers **22** and **24**. Since the semiconductor material configuration for the diodes described herein can be the same as that for HEMT devices that can be used in the same circuits, the diodes and HEMT devices can be integrated onto a single chip, as seen for example in FIGS. **5***a* and **5***b*, thereby simplifying the fabrication process and reducing cost.

Substrate **20** can be any suitable substrate upon which semiconductor layers **22** and **24** can be formed. In some embodiments, a buffer layer is included between substrate **20** and semiconductor layer **22** to minimize material defects in layers **22** and **24**. Anode contact **27**, formed upon surface **25** of layer **24**, forms a Schottky contact to layer **24**. Cathode contact **28** contacts the 2DEG in ohmic region **29**, forming a contact which is a substantially ohmic contact. Cathode contact **28** can be made to contact the 2DEG in a number of ways. For example, a metal or combination of metals can be deposited in ohmic region **29** upon surface **25** of layer **24**, followed by a thermal anneal which results in the deposited metal forming a metallic alloy with the underlying semiconductor material. Other methods by which the 2DEG can be contacted include but are not limited to ion implantation of n-type dopants into ohmic region **29**, followed by a metal deposition atop this region, or by etching away the material in ohmic region **29** and regrowing n-type material, followed by a metal deposition atop this region.

The diode in FIG. **4***a* operates as follows. When the voltage at the anode contact **27** is less than that at the cathode contact **28**, such that the Schottky junction between anode contact **27** and III-V layer **24** is reverse biased, the diode is in the OFF state with no substantial current flowing between the anode and cathode. When the voltage at the anode contact **27** is greater than that at the cathode contact **28**, as shown in FIG. **4***c*, the Schottky junction between anode contact **27** and III-V layer **24** is forward biased, and the diode is in the ON state. Electrons **5** flow from the cathode contact **28** predominantly through the 2DEG **26** and then through the forward biased Schottky junction into the anode contact **27**. That is, at least 99% of the total forward bias current flows from the anode to the cathode through the Schottky barrier and through the 2DEG channel. A small amount of leakage current can flow through other paths, such as along the surface of the device.

FIGS. **5***a* and **5***b* show a cross-sectional and plan view, respectively, of a diode **60** of the embodiment in FIG. **4***a* connected in series with a HEMT **61** integrated on the same chip. The HEMT **60** includes source and drain ohmic contacts **34** and **35**, respectively, and gate contact **36**. The HEMT can optionally include gate insulators, gate recesses, field plates, passivation layers, and other features well known in the art. The diode is connected to the HEMT by an interconnect **37**, which can be isolated from the semiconductor by including an insulator **39** between the semiconductor surface and the interconnect. In general, the interconnects connect either of the two diode terminals to any of the three HEMT terminals. The circuit schematic for the layout of FIGS. **5***a* and **5***b* is shown in FIG. **5***c*.

As used herein, the term "III-Nitride material" or "III-N material" refers to a compound semiconductor material according to the stoichiometric formula $Al_xIn_yGa_zN$, where x+y+z is about 1. For high voltage switching applications, III-Nitride (III-N) semiconductor materials are desirable for Schottky diodes due to their wide bandgap, which enables formation of devices with large breakdown voltages, as well as due to their high mobilities, which results in low on-resistance. Additionally, making use of III-N heterostructures (i.e. structures that contain at least two III-N materials with different group III compositions) that form a 2DEG to design

Schottky diodes is advantageous because the 2DEG has a much higher electron mobility than that of bulk III-N material, thereby resulting in a lower sheet resistance of the conduction path in semiconductor layer **22** than can be obtained with bulk III-N material, which results in a lower on-resistance for the diode.

In the device of FIG. **4***a*, when III-N materials are used for semiconductor layers **22** and **24**, substrate **20** can be GaN, AlN, SiC, sapphire, Si, or any other suitable substrate upon which III-N devices can be formed. III-N layers **22** and **24** are oriented in the [0 0 0 1] (C-plane) direction, but can also be oriented in a semi-polar direction and terminated by a group III element. Or, layers **22** and **24** can be oriented in a non-polar direction, such as the m-plane direction, in which case part or all of layer **24** is doped with an n-type impurity to induce the 2DEG. The compositions of III-N layers **22** and **24** are selected from the group consisting of the nitrides of gallium, indium and aluminum, and combinations thereof. However, the relative amounts of gallium, indium, and aluminum in layers **22** and **24** are different and are chosen such that the bandgap of layer **24** is larger than that of layer **22**. The polarization fields in the two layers act to induce the 2DEG **26** in layer **22**. As compared to GaN, $Al_aGa_{1-a}N$ has a larger bandgap and $In_bGa_{1-b}N$ has a smaller bandgap. In general for III-N materials, increasing the Al composition results in a larger bandgap, and increasing the In composition results in a smaller bandgap. As an example, III-N layers **22** and **24** can be GaN and $Al_aGa_{1-a}N$, respectively, where 'a' is between 1 and a finite value greater than zero, such as between about 0 and 0.3, for example between about 0.15 and 0.2. Or, as another example, III-N layers **22** and **24** can be $In_bGa_{1-b}N$ and GaN, respectively, where 'b' is between 1 and a finite value greater than zero such as between about 0 and 0.2.

Using metals with different work functions for anode contact **27** allows the Schottky barrier height to be adjusted. Examples of metals that can be used include but are not limited to Ti, Cr, NiCr, Ni, Ge, Pt, and Cu. Additionally, adjusting the composition of the upper semiconductor layer **24** not only changes the bandgap but also the semiconductor work function of this layer, thereby allowing for a second method of adjusting the Schottky barrier height. Increasing the bandgap of the upper semiconductor layer **24** also tends to increase the electron concentration in the 2DEG, which tends to reduce the diode on-resistance but can also decrease the reverse-bias breakdown voltage. Thus, an optimal value for the on-resistance can be achieved by adjusting the bandgap of layer **24** to a value resulting in the minimum breakdown voltage that can be tolerated in the particular application for which the diode is being used. Additionally, all or part of semiconductor layer **22** can be doped n-type. Doping also decreases the device on-resistance, again at the expense of potentially reducing the reverse-bias breakdown voltage, but the Schottky barrier height is unaffected.

More embodiments of this invention, shown in FIGS. **6-15**, include features such as field plates, back-side cathode contacts, recessed material underneath the anode Schottky contact, additional semiconductor layers, compositionally graded semiconductor layers, and integrated semiconductor devices, such as transistors, on the same chip. These features can be used independently or in combination with one another. Additionally, features which were optionally included in the device shown in FIG. **4***a*, such as n-type doping of one or more of the semiconductor layers, use of a semiconductor buffer layer, and adjusted Schottky barrier height obtained by varying the composition of the anode metal or the semiconductor material which the anode metal contacts, can also be included in these embodiments.

The device in FIG. **6** is similar to that of FIG. **4a**, but here the diode also includes a field plate **21** with the anode contact. The same numbers in FIGS. **4a** and **6** correspond to the same layers. Layer **23** in FIG. **6** is an insulator, such as SiN. The field plate **21** in this diode reduces the peak electric field at the edge of the anode, thereby increasing the reverse-bias breakdown voltage while having no substantial impact on the on-resistance or other on-state characteristics. In particular, slant field plates, such as those described in U.S. patent application Ser. No. 11/841,476, filed Aug. 20, 2007, are especially desirable in this application. Additionally, multiple field plate structures can be used.

The device in FIG. **7a** is similar to that of FIG. **6**, except that in this device the metallic cathode contact **28** is connected to metal layer **38** which extends to the backside of the device through vias **33**. The same numbers in FIGS. **6** and **7a** correspond to the same layers. In this device, prior to deposition of layer **23**, cathode contact **28** is deposited and region **32**, which includes portions of layers **22** and **24**, is rendered n-type or conducting, for example by a method such as ion-implantation, diffusion, or epitaxial regrowth, or by annealing the device such that cathode contact **28** forms an alloy with the semiconductor material in region **32**. In some embodiments, an n-type dopant such as Si is implanted into region **32**, and after the deposition of cathode contact **28**, the sample is annealed such that cathode contact **28** forms an alloy with the semiconductor material in region **32**, resulting in a low-resistance ohmic contact between cathode contact **28** and the material in region **32**.

Cathode contact **28** also serves as an etch stop for via **33** and can be comprised of any metal or combination of metals that results in an ohmic contact to layer **24** in region **32** and can also serve as an etch stop for the etch of via **33**. Via **33** is then etched through the back of the wafer all the way through n-type region **32** to cathode contact **28**. Alternatively, in the case where the sample is annealed such that cathode contact **28** forms an alloy with the semiconductor material in region **32**, via **33** may extend into region **32** but not all the way to the interface between region **32** and cathode contact **28**. Metal layer **38** is then deposited conformally over the backside of the wafer such that it contacts cathode contact **28** or n-type region **32** or both, resulting in the device shown in FIG. **7a**. Having a back metal for the cathode can simplify the packaging for the device.

The device in FIG. **7b** is the same as that in FIG. **7a**, except that substrate **20** is removed prior to deposition of metal layer **38**. Although this structure may be more brittle than that of FIG. **7a**, it offers the advantage that on-state current can potentially flow both laterally through the 2DEG and vertically through layer **22**, thereby reducing the device on-resistance. Additionally, the device in FIG. **7b** may exhibit better thermal properties, since substrate **20** is often comprised of a material which exhibits poor thermal conductivity.

The device in FIG. **8** is similar to that of FIG. **4a**, but here layer **24** of the diode also includes a recess **31** in layer **24** underneath a portion of the anode contact **27**. The same numbers in FIGS. **4a** and **8** correspond to the same items. The anode recess can have the same effect as a field plate, reducing the peak electric field at the edge of the anode and increasing the reverse-bias breakdown voltage. Additionally, the recess potentially reduces the series resistance from anode to cathode when the device is in the ON state, thereby reducing the on-resistance.

The device in FIG. **9a** is similar to that of FIG. **8**, but here the recess **31** extends all the way through layer **24** and through part of layer **22**. In this device, anode contact **27** directly contacts layer **22**, forming a Schottky contact with said layer.

The device also includes insulator layer **120** on top of layer **24**, with a portion **41** of the anode contact formed on top of insulator layer **120**. Insulator layer **120** can protect the surface of semiconductor layer **24** from being damaged during device fabrication. When this device is reverse biased, the reverse biased Schottky junction between anode contact **27** and layer **22** prevents current from flowing through the device. Additionally, during reverse bias operation, the portion of 2DEG **26** directly underneath portion **41** of the anode contact is depleted of electrons, thereby reducing reverse leakage currents in the device. In order for the portion of 2DEG **26** directly underneath portion **41** of the anode contact to become depleted of electrons during reverse bias operation, insulator layer **120** cannot be too thick. In some embodiments, insulator layer **120** is less than about 7 nm, less than about 5 nm, or less than about 3 nm. In some embodiments, insulator layer **120** is SiN and is deposited by metal-organic chemical vapor deposition (MOCVD). In some embodiments, insulator layer **120** also functions as a surface passivation layer. The device can also include a second insulator layer **121** on top of a portion of insulator layer **120**, as illustrated in FIG. **9b**. In the embodiment shown in FIG. **9b**, anode contact **27** extends over part of the second insulator layer **121**, thereby forming a field plate. In some embodiments, the second insulator layer **121** is SiN. In other embodiments, the device further includes a sidewall insulator **122** between anode contact **27** and the 2DEG **26**, as illustrated in FIG. **9c**. The sidewall insulator **122** can reduce reverse leakage currents. In embodiments where a sidewall insulator **122** is included, when a forward bias is applied, current flows from the anode into semiconductor layer **22** through the interface between anode contact **27** and semiconductor layer **22**, then through region **130** in semiconductor layer **22**, and then through the 2DEG to the cathode contact **28**. As illustrated in FIG. **9d**, in some embodiments, an additional III-V semiconductor layer **123**, such as AlN, is included in between layers **22** and **24**. This layer can increase the carrier mobility in the 2DEG **26**, which leads to a reduction in the forward-bias resistance of the device.

FIG. **10a** shows a diode which is similar to that shown in FIG. **4a**, but further includes a deep recess underneath the anode contact. As used herein, the term "deep recess" refers to a recess that is substantially deeper than the thickness of the second III-N layer **44**, such as at least 5 times thicker or at least 10 times thicker. This device includes a substrate **20**, a first III-N layer **42**, a second III-N layer **44**, and furthermore includes a third III-N layer **45** and an insulator **49**. A 2DEG **26** is induced in the first III-N layer **42** near the interface between layers **42** and **44**. III-N layer **45** is substantially thicker than layer **44**, such as at least 5 times thicker or at least 10 times thicker. Part or all of III-N layer **45** can be doped n-type in order to increase the conductivity of the 2DEG **26**. Insulator **49** serves as a surface passivation layer and also prevents anode contact **27** from directly contacting III-N layer **45**.

In some embodiments of this device, the first III-N layer **42** is GaN, the second III-N layer **44** is $Al_xGa_{1-x}N$, where x is about 0.27, and the third III-N layer **45** is GaN and is delta-doped with Si. The second III-N layer **44** is about 30 nm thick, and the third III-N layer **45** is about 250 nm thick. In this structure, the uppermost semiconductor surface can be substantially farther from the 2DEG than in the structures shown in FIGS. **4-8**, which can suppress surface-related effects, such as dispersion. Additionally, this device can be easily integrated with a III-N HEMT for which the III-N layer structure is similar to that of this device. FIGS. **10b** and **10c** show cross-sectional and plan views, respectively, of a diode **54** of this embodiment in series with a III-N HEMT **55**, integrated on the same chip. The HEMT **55** includes source and drain

ohmic contacts **34** and **35**, respectively, and gate contact **36**, and may optionally include features well known in the art, such as a gate insulator **53**. The diode is electrically connected to the HEMT by an interconnect **37**, which can be isolated from the semiconductor layers by including an insulator **39** between the semiconductor surfaces and the interconnect. In general, the interconnects can connect either of the two diode terminals to any of the three HEMT terminals. The circuit schematic for this layout is shown in FIG. **10**d.

FIGS. **11**a and **12**a show diodes which may be easily integrated with III-N enhancement-mode HEMT devices that were disclosed in U.S. patent application Ser. No. 12/108, 449, filed Apr. 23, 2008, which is hereby incorporated by reference throughout. It is particularly desirable to be able to integrate diodes with enhancement-mode devices, because enhancement-mode devices and diodes are commonly used together in power switching circuit applications.

The device of FIG. **11**a includes a substrate **20**, a first III-N layer **42** on the substrate **20**, a second III-N layer **44** on top of the first III-N layer, a third III-N layer **63** on top of the second III-N layer, and a fourth III-N layer **64** on top of the third III-N layer. The specific requirements for layers **42**, **44**, **63**, and **64** are the same as those of layers **94**, **98**, **95**, and **100**, respectively, in FIG. 13a of U.S. patent application Ser. No. 12/108, 449. The material of the first III-N layer **42** is selected from the group consisting of nitrides of gallium, indium and aluminum, and combinations thereof. The second III-N layer **44** is AlXN, where X is selected from the group consisting of gallium, indium or their combination. A III-N layer **63** is adjacent the AlXN layer, that includes two channel access regions. This III-N layer can be GaN, InN, or a combination of the two, preferably GaN. In one embodiment of this device, layer **64** is $Al_mGa_{1-m}N$ and is used for enabling the 2DEG charge in the channel access regions. The exact compositions of layers **42**, **44**, **63**, and **64** are chosen such that a 2DEG **26** is induced in III-N layer **63** near the interface between layers **63** and **64**, as described in U.S. patent application Ser. No. 12/108,449. The device also includes an anode Schottky contact **27** or a plurality of contacts atop layer **64**, and a cathode contact **28** or plurality of contacts contacting the 2DEG **26**. In one embodiment of this device, layer **42** is GaN, layer **44** is $Al_xGa_{1-x}N$, where x is in the range of about 0.05 to 0.25 and layer **44** is about 5-10 nm thick, layer **63** is GaN and is about 5-30 nm thick, and layer **64** is $Al_mGa_{1-m}N$, where m is in the range of about 0.1 to 0.3 and the thickness of the layer **64** is in the range of about 10-50 nm, the composition and thickness ranges being selected to achieve an equivalent sheet resistance of under 700 ohms/square in the 2DEG region. FIGS. **11**b and **11**c show cross-sectional and plan views, respectively, of the diode of FIG. **11**a **69** integrated with an enhancement-mode HEMT **88**, and FIG. **11**d shows a circuit schematic of this configuration. In FIGS. **11**b and **11**c, layers **39** and **86** are insulators such as SiN.

The device of FIG. **12**a includes a substrate **20**, a first III-N layer **42** on the substrate, a second III-N layer **72** on top of the first III-N layer, a third III-N layer **73** on top of the second III-N layer, and a fourth III-N layer **74** on top of the third III-N layer. The specific requirements for layers **42**, **72**, **73**, and **74** are the same as those of layers **94**, **98**, **95**, and **100**, respectively, in FIG. 14a of U.S. patent application Ser. No. 12/108, 449. The exact compositions of layers **42**, **72**, **73**, and **74** are chosen such that a 2DEG **26** is induced in III-N layer **73** near the interface between layers **73** and **74** and a 2DEG **26** is induced in III-N layer **42** near the interface between layers **42** and **72**, as described in U.S. patent application Ser. No. 12/108,449. The device also includes an anode Schottky contact **27** or a plurality of contacts atop layer **74**, and a cathode

contact **28** or plurality of contacts contacting the 2DEG **26** in layer **73**. The cathode contact **28** can optionally also contact the 2DEG **26** in layer **42**, as shown. In order for a 2DEG **26** to be induced in layer **42**, the Al composition and/or thickness of III-N layer **72** is greater than that of layer **44** in FIG. **11**a if layers **42**, **73**, and **74** in FIG. **12**a have the same thicknesses and compositions as FIGS. **42**, **63**, and **64**, respectively, in FIG. **11**a. FIGS. **12**b and **12**c show cross-sectional and plan views, respectively, of the diode of FIG. **12**a **79** integrated with an enhancement-mode HEMT **98**, and FIG. **12**d shows a circuit schematic of this configuration.

The device shown in FIG. **13** is similar to that shown in FIG. **12**a, but here a portion of the semiconductor material underneath the anode contact **27** is recessed, such that the recess terminates inside III-N layer **42**. In this device, anode contact **27** directly contacts layers **42**, **72**, **73**, and **74**, forming Schottky contacts with layers **42** and **73**. In some embodiments, the device also includes insulator layer **124** on top of layer **74**, with a portion of the anode contact formed on top of insulator layer **124**. In some embodiments, insulator layer **124** is SiN. In some embodiments, the device also includes a sidewall insulator in the anode recess (not shown), similar to layer **122** in FIG. **9**c. In other embodiments, the device includes an additional III-N layer, such as AlN, between layers **73** and **74** (not shown).

FIGS. **14**a-**14**b show embodiments of this invention that include compositionally graded III-N layers. For an $Al_xGa_{1-x}N$ layer oriented in the polar [0 0 0 1] direction or in a semi-polar Ga-terminated orientation, if x is not constant throughout the layer but rather monotonically increases from the bottom of the layer (N-polar face) to the top of the layer (Ga-polar face), the polarization fields in the layer cause it to be doped n-type. This is known as polarization doping, and the resulting doping profile is a 3-dimensional distribution sometimes referred to as a 3-dimensional electron gas, or 3DEG. The exact doping profile in the layer is determined by the grading profile of x. For example, a linear grade for x results in an approximately constant doping throughout the layer. Other grading profiles, such as exponential grades or parabolic grades, result in different doping profiles. A similar effect may be achieved by grading $In_yGa_{1-y}N$. In this case, if y decreases monotonically from the N-polar face to the Ga-polar face, the polarization fields in the layer cause it to be doped n-type.

The diode in FIG. **14**a includes a substrate **20**, on top of which is formed a III-N layer **42**, on top of which is formed a compositionally graded III-N layer **104** which contains a channel consisting of a polarization-induced charge distribution. III-N layer **104** is graded to induce n-type conductivity within the layer, as was described above. In some cases, the III-N materials are oriented in the polar [0 0 0 1] direction or in a semi-polar Ga-terminated orientation. Depending on the grading profile in III-N layer **104**, the channel is distributed over the entire layer **104**, or is only distributed over a portion of layer **104**. An anode Schottky contact **27** or plurality of contacts is formed atop layer **104**, and a cathode contact **28** or plurality of contacts is formed that makes a significantly ohmic contact with the polarization-induced channel in layer **104**. In some implementations of this embodiment, III-N layer **42** is GaN, either semi-insulating or n-doped or n-doped, and III-N layer **104** is $Al_xGa_{1-x}N$, where x is about zero at the interface of layers **102** and **104** and increases monotonically up to the upper surface of layer **104**. In some embodiments, at the upper surface of layer **104**, x is between about 0.1 and 0.3. One of the advantages to this structure is that the composition of the upper surface of the upper III-N

layer **104** can be more easily adjusted to obtain different Schottky barrier heights while still resulting in a highly conductive channel in layer **104**.

The diode in FIG. **14**b is similar to that in FIG. **14**a, but further includes an additional III-N layer **106** atop layer **104** but below anode contact **27**. When layer **104** is $Al_xGa_{1-x}N$ and is graded as described above, III-N layer **106** is GaN or $Al_zGa_{1-z}N$. In some applications, z is larger than the maximum value of x, thereby resulting in an additional 2-dimensional charge distribution (2DEG) in layer **104**, which increases the conductivity of that layer and thereby may reduce the diode on-resistance. In other applications, z is less than the maximum value of x, possibly even zero, thereby reducing the diode Schottky barrier height. The devices in FIGS. **14**a and **14**b can both be modified to include a backside cathode contact, such as shown for the devices in FIGS. **7**a and **7**b.

The diode in FIG. **14**c is similar to that in FIG. **14**a, but here a portion of the semiconductor material underneath the anode contact **27** is recessed, such that the recess terminates inside III-N layer **42**. In some embodiments, the device also includes insulator layer **124** on top of layer **104**, with a portion of the anode contact formed on top of insulator layer **124**. In some embodiments, insulator layer **124** is SiN.

FIG. **15**a shows a cross-sectional view of a diode which is fabricated on III-N semiconductor material that is either oriented in the N-polar [0 0 0 1 bar] direction or is a nitrogen-terminated semipolar material. A plan view of this device is shown in FIG. **15**b. The device includes a substrate **110** which is suitable for growth of N-polar or semipolar III-N materials. Layer **112** is a buffer layer, such as GaN, which reduces the defect density in the overlying material. In some cases, it is possible to omit layer **112** and grow layer **113** directly on the substrate. The compositions of layers **113**, **114**, and **115** are chosen such that a 2DEG **26** is induced in layer **114** near the interface between layers **113** and **114**. In some embodiments, 2DEG **26** can be induced by choosing III-N materials for layers **113** and **115** which have larger bandgaps than that of layer **114**. In some embodiments, layer **113** is $Al_mGa_{1-m}N$, where 'm' is between about 0.25 and 0.35, layer **114** is GaN, and layer **115** is $Al_rGa_{1-r}N$, where 'r' is between about 0.25 and 0.35. The device can also be designed with a backside cathode contact, similar to the structure shown in FIGS. **7**a and **7**b. The diode can also be integrated with other devices, such as III-N HEMTs. The structure shown in FIG. **15**a can be advantageous as compared to other Schottky diodes because reverse bias barrier lowering is reduced, thereby reducing the reverse leakage currents in the device.

For the device in FIG. **15**a, a band diagram along line **118** when anode contact **27** and cathode contact **28** are at the same voltage is shown in FIG. **16**a, and FIG. **16**b shows a band diagram along this line when the diode is reverse biased, i.e., anode contact **27** is at a lower voltage than the cathode contact **28**. For these band diagrams, $Al_mGa_{1-m}N$ layer **113** is 30 nm thick with Al composition m=0.3, GaN layer **114** is 30 nm thick, and $Al_rGa_{1-r}N$ layer **115** is 5 nm thick with Al composition r=0.3. In this structure, the electric field in layer **115** opposes electron reverse leakage flow. When a reverse bias is applied (FIG. **16**b), the electric field in layer **115** is decreased, and so the Schottky barrier height Φ_B remains about the same, or is not substantially reduced, as compared to the case when anode contact **27** and cathode contact **28** are at the same voltage (FIG. **16**a). For example, when the device is reverse biased such that the maximum electric field E_{max} in the device is greater than about $(0.5)*E_{br}$, where E_{br} is the breakdown field of the material, the Schottky barrier height Φ_B may be reduced by less than 15%, less than 10%, less than 5%, or less

than 1% of its value when zero bias is applied. Consequently, barrier lowering in this structure can be suppressed as compared to the structure in FIG. **1**, and so reverse leakage currents can be reduced.

Furthermore, layer **113** can be doped to induce further charge at the interface between layers **113** and **114**. The doping in layer **113** can be used to keep the valence band of layers **112** and **113** away from the Fermi level to prevent dispersion. In addition to the doping, the aluminum composition of layer **113** can also be graded to keep the valence band of layers **112** and **113** away from the Fermi level. Additionally, the doping profile in layer **113** can be designed such that only the bottom part of layer **113** is doped, while the portion of layer **113** adjacent to layer **114** is not doped, in order to prevent impurity scattering at the interface between layers **113** and **114**. More details of the doping and grading designs for these layers can be found in U.S. application Ser. No. 11/523,286, filed Sep. 18, 2006.

What is claimed is:

1. An assembly comprising:
   a diode comprising a first III-N material layer; a second material layer on the first III-N material layer, wherein a 2DEG channel is in the first III-N material layer because of a compositional difference between the first III-N material layer and the second III-N material layer; and two terminals, wherein a first terminal is an anode consisting of a Schottky contact formed with the second III-N material layer and a second terminal is a single cathode in ohmic contact with the 2DEG channel; and
   a III-N transistor having a terminal,
   wherein a terminal of the two terminals of the diode is electrically connected to the terminal of the III-N transistor.

2. The assembly of claim **1**, wherein when the diode is forward biased, current flows from the anode to the cathode predominantly through a Schottky barrier and the 2DEG channel.

3. The assembly of claim **1**, wherein the first III-N material layer of the diode includes GaN.

4. The assembly of claim **1**, wherein the second III-N material layer of the diode is recessed in a location corresponding to the anode.

5. The assembly of claim **1**, wherein the diode further comprises a field plate electrically connected to the anode.

6. The assembly of claim **5**, wherein the diode further comprises an insulating layer surrounding the anode and between the field plate and the second III-N material layer.

7. The assembly of claim **1**, wherein the diode further comprises a backside electrically conductive layer, and wherein:
   the second III-N material layer of the diode includes a recess in which the backside electrically conductive layer electrically contacts the cathode.

8. The assembly of claim **7**, wherein a region of the second III-N material layer of the diode is n-type, the region contacting the cathode and the conductive layer of the diode.

9. The assembly of claim **1**, wherein the diode further comprises:
   a third III-N material layer on a side of the second III-N material layer opposite to the first III-N material layer; and
   an insulator layer on the third III-N material layer opposite to the second III-N material layer, wherein the third III-N material layer is at least five times thicker than the second III-N material layer and is doped, and the anode is in a recess in the third III-N material layer and the insulator layer.

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10. The assembly of claim **9**, wherein the terminal of the III-N transistor is a drain terminal, and the anode of the diode is electrically connected to the drain terminal of the III-N transistor.

11. The assembly of claim **9**, wherein the diode and the III-N transistor are on a common substrate.

12. The assembly of claim **1**, wherein the terminal of the III-N transistor is a drain terminal, and the anode of the diode is electrically connected to the drain terminal of the III-N transistor.

13. The assembly of claim **1**, wherein the diode and the III-N transistor are on a common substrate.

14. The assembly of claim **1**, wherein the III-N transistor is an enhancement mode III-N transistor.

15. The assembly of claim **1**, wherein the diode further comprises:

a third III-N material layer, wherein the first III-N material layer is between the second III-N material layer and the third III-N material layer and the third III-N material layer differs in composition from the first III-N material layer; and

a fourth III-N material layer, wherein the third III-N material layer is between the first III-N material layer and the fourth III-N material layer and fourth III-N material layer differs in composition from the third III-N material layer.

16. The assembly of claim **15**, wherein a second 2DEG channel is induced in the fourth III-N material layer adjacent to the third III-N material layer.

17. The assembly of claim **16**, wherein the III-N transistor is an enhancement mode III-N transistor.

18. The assembly of claim **16**, wherein the terminal of the III-N transistor is a drain terminal, and the anode of the diode is electrically connected to the drain terminal of the III-N transistor.

19. The assembly of claim **16**, wherein the diode and the III-N transistor are on a common substrate.

20. The assembly of claim **15**, wherein the III-N transistor is an enhancement mode III-N transistor.

21. The assembly of claim **15**, wherein the terminal of the III-N transistor is a drain terminal, and the anode of the diode is electrically connected to the drain terminal of the III-N transistor.

22. The assembly of claim **15**, wherein the diode and the III-N transistor are on a common substrate.

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CERTIFICATE OF CORRECTION

PATENT NO.   : 7,898,004 B2   Page 1 of 2
APPLICATION NO.   : 12/332284
DATED   : March 1, 2011
INVENTOR(S)   : Yifeng Wu and Rongming Chu

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Cover Page, (75) Inventors, please replace:

"Yifeng Wu, Goleta, CA (US);
Umesh Mishra, Montecito, CA (US);
Primit Parikh, Goleta, CA (US);
Rongming Chu, Goleta, CA (US);
Ilan Ben-Yaacov, Goleta, CA (US);
Likun Shen, Goleta, CA (US)"

with

-- Yifeng Wu, Goleta, CA (US);
Rongming Chu, Goleta, CA (US) --

On the Cover Page, (56) References Cited, Other Publications, Column 2, at line 1, please replace:

"Wanjun Chen et al., "High-performance A1Gan/Gan lateral field-""
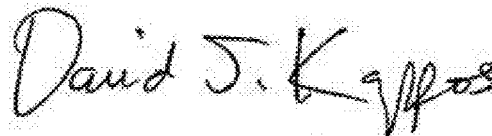
with

-- Wanjun Chen et al., "High-performance AlGan/Gan lateral field- --

On the Cover Page, (56) References Cited, Other Publications, Column 2, at line 10, please replace:

"Based High Electron Mobility Tranistors With Integrated Slant Field"

with

Signed and Sealed this
Twelfth Day of July, 2011

David J. Kappos
Director of the United States Patent and Trademark Office

-- Based High Electron Mobility Transistors With Integrated Slant Field --