UNIVERSITY of CALIFORNIA
Santa Barbara

AlGaN / GaN Current Aperture Vertical Electron Transistors

A dissertation submitted in partial satisfaction of the
requirements for the degree of

Doctor of Philosophy

in

Electrical and Computer Engineering

by

Ilan Ben-Yaacov

Committee in charge:

Professor Umesh K. Mishra, Chair
Professor Steven P. DenBaars
Professor Evelyn L. Hu
Dr. Stacia Keller

March 2004

The dissertation of Ilan Ben-Yaacov is approved:

_____

_____

_____

_____

Chair

March 2004

AlGaN / GaN Current Aperture Vertical Electron Transistors

by

Ilan Ben-Yaacov

Curriculum Vitæ

Ilan Ben-Yaacov

EDUCATION

Bachelor of Science in Physics, University of California, Santa Barbara, March 1999.

Master of Science in Electrical and Computer Engineering, University of California, Santa Barbara, June 2002.

Doctor of Philosophy in Electrical Engineering, University of California, Santa Barbara, February 2004 (expected).

PROFESSIONAL EMPLOYMENT

June 1996 - September 1996, Summer research student, Stanford Linear Accelerator Center, Stanford, CA.

February 1998 - September 1998, Senior thesis research project, University of Canterbury, New Zealand.

January 1999 - June 1999, Physics and math tutor, University of California, Santa Barbara.

September 1999 - February 2004, Research assistant, Department of Electrical and Computer Engineering, University of California, Santa Barbara.

PUBLICATIONS

I. Ben-Yaacov, Y.-K. Seck, S. P. DenBaars, and U. K. Mishra. AlGaN/GaN current aperture vertical electron transistors (CAVETs) with regrown channels. *Journal of Applied Physics*, 95(5), 2004.

I. Ben-Yaacov, Y.-K. Seck, S. P. DenBaars, E. L. Hu, and U. K. Mishra. Analysis of Leakage Currents in AlGaN/GaN Current Aperture Vertical Electron Transistors (CAVETs). *MRS Proceedings*, 764, April 2003.

Y. Gao, A. R. Stonas, **I. Ben-Yaacov**, U. K. Mishra, S. P. DenBaars, and E. L. Hu. AlGaN/GaN current aperture vertical electron transistors fabricated by photoelectrochemical wet etching. *Electronics Letters*, 39(1):148–9, 2003.

I. Ben-Yaacov, Y.-K. Seck, S. Heikman, S. P. DenBaars, and U. K. Mishra. AlGaN/GaN current aperture vertical electron transistors. pages 31–2, 2002. 60th DRC. Device Research Conference.

S. Keller, S. Heikman, **I. Ben-Yaacov**, L. Shen, S. P. DenBaars, and U. K. Mishra. Indium surfactant assisted growth of AlN/GaN heterostructures by metal-organic chemical vapor deposition. *Physica Status Solidi A*, 188(2):775–8, 2001.

S. Keller, S. Heikman, **I. Ben-Yaacov**, L. Shen, S. P. DenBaars, and U. K. Mishra. Indium-surfactant-assisted growth of high-mobility AlN/GaN multilayer structures by metalorganic chemical vapor deposition. *Applied Physics Letters*, 79(2):3449–51, 2001.

S. Keller, **I. Ben-Yaacov**, S. P. Denbaar, and U. K. Mishra. Flow modulation epitaxy of InN/GaN heterostructures; towards InN based HEMTs. pages 233–6, 2000. Proceedings of the International Workshop on Nitride Semiconductors.

R. Cheung, S. Withanage, R. J. Reeves, S. A. Brown, **I. Ben-Yaacov**, C. Kirchner, and M. Kamp. Reactive ion etch-induced effects on the near-band-edge luminescence in GaN. *Applied Physics Letters*, 74(21):3185–7, 1999.

S. A. Brown, R. J. Reeves, R. Cheung, **I. Ben-Yaacov**, S. Withanage, M. Schauler, and M. Kamp. Optical Study of Dry Etched III-Nitride Semiconductors. 1999. 23rd Australian and New Zealand Institute of Physics Condensed Matter Physics Conference.

Ilan Ben-Yaacov. *Effects of Chemical Etching on Optical Properties of GaN*. Honors thesis, University of Canterbury, Christchurch, New Zealand, 1998.

I. Ben-Yaacov, C. H. Back, and R. E. Kirby. Atomic Force Microscopy Study of High Electric Field Breakdown Through Thin Oxide Layers on Copper. 1996. 19th Surface/Interface Research Meeting, NCCAS.

Abstract

AlGaN / GaN Current Aperture Vertical Electron Transistors

by

Ilan Ben-Yaacov

During the past few years, enormous progress has been made in the development of III-nitride semiconductor materials for electronics applications. The AlGaN/GaN current aperture vertical electron transistor was proposed for its potential advantages in high-voltage switching applications as well as in high power electronics. The motivation behind development of CAVETs is twofold. First, because there is no exposed AlGaN surface on the drain side of the gate, the DC-RF dispersion commonly observed in GaN HEMTs should be mitigated. Second, because the drain is located underneath the gate, the peak electric field in a CAVET should be greatly reduced as compared to that of a HEMT. This dissertation focuses on efforts to develop growth and fabrication technology for GaN-based CAVETs.

A CAVET consists of a source region separated from a drain region by an insulating layer containing a narrow aperture that is filled with conducting material. The source is comprised of a two-dimensional electron gas formed in the GaN near the AlGaN/GaN heterointerface, while the drain consists of n-type GaN. Source contacts are deposited on either side of the aperture, while the drain metal contacts the n-doped region below the aperture. Electrons flow from the source contacts along the 2DEG, then through the aperture into the underlying GaN and are collected at the drain. A Schottky gate, located above the aperture, modulates the charge in the 2DEG, thereby controlling how much current passes through the aperture and into the drain.

Major progress has been made in identifying major issues in the DC and RF performance of AlGaN/GaN CAVETs. Devices with regrown source regions were fabricated with both Fe-doped and Mg-doped insulating layers as well as with ion implanted layers. Device I–V characteristics were obtained, and source-drain currents as high as 0.8 A/mm were demonstrated. DC-RF dispersion was indeed mitigated, and by varying the position of the gate metal relative to the aperture, the effects of the AlGaN surface on dispersion were clearly observed. An analysis of leakage currents was carried out, and source leakage was

successfully eliminated. Finally, small signal RF measurements were conducted, and an f_τ of over 12 GHz was demonstrated.

Contents

List of Figures

List of Tables

Acknowledgements

WORKING at UC Santa Barbara has been an incredibly rewarding experience. I believe UCSB to be a unique university in the sense that the sharing of ideas and knowledge extends not only beyond individual groups but also between departments. I had the opportunity to work with and exchange ideas and information with people from the electrical engineering, materials, chemistry, and physics departments.

I began my undegraduate work here in 1994, then my graduate work in 1999, and throughout that time I have had the opportunity to work with many outstanding researchers. First and foremost, I am extremely grateful to have worked for my advisor, Prof. Umesh Mishra. Umesh has assembled a research environment in which all group members work together and are constantly providing support for one another. He also gives his graduate students the freedom to pursue their own ideas, and he has provided valuable technical guidance over the years and has been a good friend. In addition, the other members of my PhD committee played a vital role in my research experience. Prof. Steve DenBaars brought me into the MOCVD group and gave me the opportunity to be an MOCVD grower, and he has provided valuable input with regards to material issues in my devices. Dr. Stacia Keller taught me how to grow by MOCVD, and in my opinion is the best resource in the world for any technical issues regarding MOCVD of GaN. Prof. Evelyn Hu has been a valuable resource in helping me understand processing issues for devices.

Over the years, I have benefited from working with a large number of fellow researchers. First off, I would like to thank the other members of the GaN CAVET group at UCSB, Yan Gao and Yee-Kwang Seck. Since Yan and I were (to the best of my knowledge) the only two people on the planet processing GaN CAVETs, we spent a lot of time comparing data and coming up with new ideas. Yee-Kwang performed all of the CAVET simulations on ATLAS and helped us all understand the fundemental principles of CAVET operation. I would also particularly like to thank Sten Heikman for the guidance he has given me in both growth and processing. A number of the growth and processing techniques implemented in CAVET fabrication were originally developed by Sten. I am grateful to Naiqian, Rob, and Dario for teaching me how to process, to Siddarth and Tomas for help with RF measurements, and to Likun, Ale, and

Huili for additional help in processing and growth. I would also like to acknowledge some of the other members of Profs. Mishra, York, and DenBaars groups who I have worked with either in the office, cleanroom, or MOCVD lab: Arpan, Birgit, Can, Dan G., DJ, Gia, Haijiang, James, Jeff, Lee, Mike G., Peter, Rama, Yingda, Chris, Nadia, Paolo, Andreas, Brendan, Craig, Mike C., Monica, Pablo, Paul, Tal, and Tom. The Mishra group would probably cease to exhist as we know it if it weren't for the support of Umesh's administrative assistants Lee B., Cathy, Masika, Emeka, Laura, and Pam. I would like to thank Val de Veyra in the ECE graduate student office for always pointing me in the right direction. Jack, Bob, Neil, Brian T., Don, and Ning have done a fabulous job keeping the cleanroom running smoothly over the years, none of the research that we do would be possible without them. I would also like to thank Brian C. and Mike I. in the MOCVD lab, Youli in the X-ray lab, and Mark and Jin-Ping in the microscopy lab.

I would also like to acknowledge financial support from an NDSEG fellowship provided by the Department of Defense (DoD) as well as additional support from the Air Force Office of Scientific Research (AFOSR) and the Office of Naval Research (ONR).

Finally, I would like to acknowledge the support of all my friends and family. Thanks to the J-crew Lowy, Ruskin, Bryce, Gil, Ethan, Kevin, Laura, Amy, and Jake. Thanks to my climbing crew Olav, Johnnie Love, Orlando, Enzo, and Jerry. Thanks to my current and past housemates, Nathalie, Jeanine, and to SBOCC. Thanks to my parents, my sisters Ronit and Tammy, and my brother-in-law Scott for their endless support. And of coarse, thanks to my girlfriend Vicky for her support and understanding.

Dedicated to my grandmother, Rosa Ozdoba

(1916 - 2003)

1 Introduction

DURING the past few years, enormous progress has been made in the development of Gallium Nitride (GaN) and its family of material alloys for both optoelectronics and electronics applications. With the commercialization of GaN-based LEDs [1] and laser diodes [2], as well as recent developments in UV detectors [3], GaN will continue to play an important role in visible wavelength and UV optoelectronics. For electronics applications, there exist a number of devices that take advantage of both the high critical breakdown fields associated with the large bandgap of GaN as well as its high saturated electron velocities. These devices are intended to fulfill the growing demands for high power, high frequency electronic components as well as for high voltage power switches. Impressive demonstrations of AlGaN/GaN high electron mobility transistors (HEMTs) [4] and heterojunction bipolar transistors (HBTs) [5]

continue to be reported, and microwave GaN HEMTs are nearing commercialization.

This dissertation will focus on the development of GaN-based current aperture vertical electron transistors (CAVETs). Although similar structures have been used for electronic devices in other material systems [6], the CAVET structure had previously never been explored for III-nitride technology. As the initial effort at UCSB to fabricate GaN CAVETs, the primary focus of the work was to develop the material growth and processing techniques required for device fabrication, demonstrate working devices, and analyze the electrical characteristics of these devices. Additionally, a basic theoretical device model was developed to describe fundamental aspects of device operation, and a small-signal RF analysis was conducted. As a whole, the work has also contributed to the overall understanding of GaN field effect transistors, and a number of the techniques developed for the growth and fabrication of CAVETs could potentially be beneficial in other areas of GaN technology.

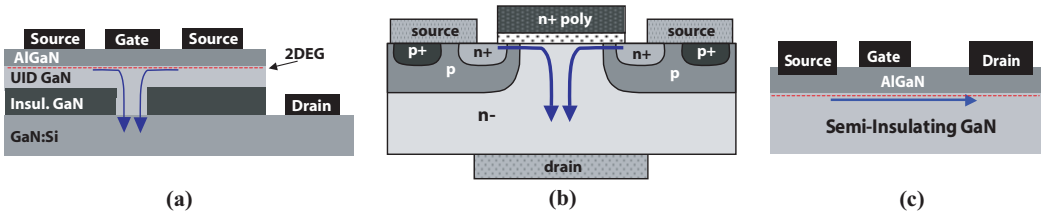

Figure 1.1: Schematic diagram of (a) GaN-based Current Aperture Vertical Electron Transistor (CAVET), (b) DMOS structure, and (c) GaN HEMT.

1.1 Motivation for the development of AlGaN/GaN CAVETs

The AlGaN/GaN CAVET was proposed for its potential advantages in high voltage, high power, and high temperature electronics applications, especially in high voltage power switching. The two most important requirements for switching devices are a large breakdown voltage V_{BR} and a low on-resistance R_{on}. Silicon has long been the dominant semiconductor for high voltage power switching devices, most commonly making use of the double-diffused metal-oxide-semiconductor (DMOS) structure [7], which is illustrated in Figure 1.1(b). However, silicon power devices are rapidly approaching theoretical limits for performance. At the same time, wide bandgap materials, particularly GaN and SiC, have been attracting much attention because they offer a number of potential

advantages over silicon. These potential advantages arise from the fundamental physical properties of the material. GaN has projected saturated electron velocities of 2.5×10^7 cm/s [8] and a 3.4 eV bandgap that leads to a critical breakdown field of 3.3 MV/cm, as well as stability at high temperatures. Additionally, the ability to form AlGaN/GaN heterojunctions, which result in a two-dimensional electron gas (2DEG) in the GaN near the AlGaN/GaN heterointerface, allows for very high electron mobilities μ_n while maintaining a large channel charge n_s. Large $\mu_n{\cdot}n_s$ products in devices result in low on-resistances R_{on}. The GaN HEMT, which takes advantage of these attributes, is illustrated in Figure 1.1(c). Table 1.1 compares some of the fundamental physical properties of GaN to those of other major semiconductors.

The high breakdown field strength in GaN permits very high voltages to be sustained during operation of GaN-based devices. In HEMTs, breakdown results from an avalanche process that usually occurs near the gate edge on the drain side, where accumulation of charge at high gate-drain voltages results in large localized electric fields. Achieving a high breakdown voltage in a HEMT requires decreasing the electric field at the surface of the channel at the drain edge of the gate. In GaN HEMTs, this has been accomplished by Zhang *et al.*

Property	*Si*	*GaN*	*AlN*	*4H-SiC*	*Diamond*
E_g [eV]	1.1	3.39	6.1	3.26	5.45
n_i [cm^{-3}]	1.5×10^{10}	1.9×10^{-10}	$\sim10^{-31}$	8.2×10^{-9}	1.6×10^{-27}
ε_r	11.8	9.0	8.4	10	5.5
μ_n [cm^2/V·s]	1350	1500	1100	700	1900
v_{sat} [10^7 cm/s]	1.0	2.5	1.8	2.0	2.7
E_{crit} [MV/cm]	0.3	3.3	11.7	3	5.6
Θ_K [W/cm·K]	1.5	1.3	2.5	4.5	20

Table 1.1: Physical properties of various semiconductors relevant to high-voltage applications

with the employment of an insulated gate structure, and source-drain breakdown voltages of over 1 kV have been achieved [9]. Another promising approach to achieving bulk breakdown limits in nitride-based electronic devices is to employ a CAVET structure.

A CAVET, which is illustrated in Figure 1.1(a), is the GaN analogue of the Si DMOS structure. A CAVET consists of a source region separated from a drain region by an insulating layer containing a narrow aperture that is filled with conducting material. The source region is comprised of a two-dimensional electron gas (2DEG) formed in the GaN near the AlGaN/GaN heterointerface, while the drain region consists of n-type GaN. A device mesa is formed by reactive ion

etching (RIE), and source contacts are deposited on either side of the aperture. The drain metal contacts the n-doped region below the aperture. Electrons flow from the source contacts along the 2DEG, then through the aperture into the n-type GaN and are collected at the drain. The conductivity of the material inside the aperture as well as in the drain region must be much larger than that of the 2DEG so that the total current passing through the device is determined by the conductivity of the 2DEG. Simultaneously, the conductivity of the 2DEG must be much higher than that of the adjacent bulk GaN directly below the 2DEG to ensure current flow through the 2DEG rather than through the bulk GaN. A Schottky gate, located directly above the aperture, is used to modulate the charge in the 2DEG, thereby controlling how much current passes through the aperture and is collected at the drain.

The AlGaN/GaN CAVET combines the attributes of both the DMOS and the GaN HEMT into a single device. The high conductivity in the 2DEG results in a low on-resistance. Additionally, because the virtual drain (or the pinched off region) is located underneath the gate, charge does not accumulate at the gate edge, so no large fields near the gate edge are present. Instead, our simulations show that the electric field distribution in a CAVET is similar to that of a DMOS; the

high field region is buried in the bulk below the gate metal. The CAVET therefore has the potential to support very large source-drain voltages, since surface related breakdown is eliminated. An additional benefit from this sort of field distribution is that surface related instabilities such as DC-RF dispersion, which present serious problems in GaN HEMTs, are mitigated in a CAVET.

1.2 Research background of GaN-based transistors

As compared to many other material systems, research on electronic devices in the III-Nitrides is relatively immature. The majority of research on GaN electronic devices has focused on high electron mobility transistors (HEMTs), although more recently a number of groups have also reported AlGaN/GaN heterojunction bipolar transistors (HBTs) and current aperture vertical electron transistors (CAVETs).

The first significant achievement in GaN HEMT technology was the observation of a two dimensional electron gas formed by an AlGaN/GaN heterojunction, which was reported by Khan *et al.* in 1992 [10]. The following year, Khan *et al.* reported the first DC performance of a GaN MESFET [11]. In 1994, the first small signal measurements of a GaN MESFET [12] and an AlGaN/GaN

HEMT [13] were reported. Then in 1996, Wu *et al.* reported the first measured microwave power of 1.1 W/mm at 2 GHz [14] in a GaN HEMT. Not too long after, the first X-band power of 0.27 W/mm was reported [15]. Since 1996, the power density reported for GaN HEMTs has increased dramatically, and power densities as large as 30 W/mm at 8 GHz were recently reported [16].

Work on GaN bipolar transistors began later, with the first AlGaN/GaN HBT reported in 1998 [17]. Shortly after, Yoshida *et al.* demonstrated HBTs with common emitter current gains greater than 10 [18]. In 1999, Limb *et al.* reported improved HBTs in which the emitters were selectively regrown [19]. More recently, HBTs with current gains as high as 35 at 300 K were reported by Xing *et al.* [20], and the temperature dependence of the current gain and common emitter offset voltage was studied by Huang *et al.* [21].

To date, a very small number of reports of CAVETs have been published. At the time of publication, only two groups, both at UCSB, had demonstrated AlGaN/GaN CAVETs. The first CAVETs, which contained regrown aperture and source regions, were completed in 2001 [22] (see § 3.2). Soon after, reports were published of CAVETs in which the insulating region was formed by a photoelectrical chemical (PEC) etch of an InGaN layer [23]. Other publications

include the fabrication of CAVETs with higher drain currents and very little dispersion [24] as well as an analysis of parasitic leakage currents and DC-RF dispersion [25].

1.3 Synopsis of the dissertation

This dissertation focuses on the development of the AlGaN/GaN CAVET for microwave power as well as high voltage switching applications. For a high voltage switch, the primary objective is the demonstration of a device with both a very large breakdown voltage and a low on-resistance, while for a microwave transistor, the end goal is demonstrating RF power performance. Because a CAVET had never been previously reported, the majority of this work was focused on development of the device process as well as gaining an understanding of device operation and the parameters that affect device performance.

Chapter 2 provides the foundation of this thesis by describing the device modeling, material growth, and fabrication of the CAVET. A theoretical model is developed which accurately predicts device performance, and material growth and processing techniques are introduced. MOCVD regrowth was critical for

the fabrication of devices and is described in § 2.5.2. Critical design parameters are identified, and various device layouts used in this work are discussed.

In Chapter 3, device characteristics of the first CAVETs are presented. I-V curves for devices with both Fe- and Mg-doped insulating layers are shown. Also included is an analysis of DC-RF dispersion. Dispersion was explicitly shown to result from AlGaN surface states and was mitigated in devices where the gate completely covered the aperture region.

In Chapter 4, a complete analysis of parasitic leakage currents in a CAVET is conducted. Three active leakage paths are identified, and methods to independently quantify the leakage through each path are presented. Techniques to eliminate leakage are discussed, and devices are presented for which leakage through the insulating layer has been eliminated.

Chapter 5 presents results for CAVETs in which the insulating layer is defined by an aluminum ion implantation. A significant reduction in leakage is achieved while maintaining very large drain currents. Also discussed is ion implantation in GaN, especially for the purpose of electrical isolation, as well as regrowth on implanted layers.

Finally, in Chapter 6, device small signal RF measurements are presented.

The gate-overlap length L_{go} was shown to be the primary factor in determining the current gain cutoff frequency f_τ. However, an additional delay was also measured, which was attributed to a combination of drain delay as well as the channel extending beyond the edge of the aperture before pinching off. In addition, DC measurements of devices with varying values of L_{go} were performed to determine the minimum value of L_{go} that can be achieved before DC performance degrades.

References

[1] S. Nakamura, M. Senoh, N. Iwasa, S. Nagahama, T. Yamada, and T. Mukai. Superbright Green InGaN Single-Quantum-Well-Structure Light-Emitting Diodes. *Jpn. J. Appl. Phys., Part 2*, 34:L1332–5, 1995.

[2] S. Nakamura, M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, and Y. Sugimoto. InGaN-Based Multi-Quantum-Well-Structure Laser Diodes. *Jpn. J. Appl. Phys., Part 2*, 35:L74–6, 1996.

[3] B. Poti, M. T. Todaro, M. C. Frassanito, A. Pomarico, A. Passaseo, M. Lomascolo, R. Cingolani, and M. De Vittorio. High responsivity GaN-based UV detectors. *Electronics Letters*, 39(24):1747–9, 2003.

[4] Robert Coffie. *Characterizing and Suppressing DC-to-RF Dispersion in AlGaN/GaN High Electron Mobility Transistors*. PhD thesis, University of California, Santa Barbara, 2003.

[5] H. Xing, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra. High current gain GaN bipolar junction transistors with regrown emitters. *Proceedings of the IEEE Twenty-Seventh International Symposium on Compound Semiconductors*, pages 365–9, 2000.

[6] J. B. Casady, A. K. Agarwal, L. B. Rowland, W. F. Valek, and C. D. Brandt. 900 V DMOS and 1100 V UMOS 4H-SiC power FETs. *55th Annual Device Research Conference Digest*, pages 32–3, 1997.

[7] B. Metzger. LDMOS turns up the power. *Compound Semiconductor*, 8(5):33, 2002.

[8] O. Ambacher. Growth and applications of group III-nitrides. *Journal of Physics D*, 31(20):2653–710, 1998.

[9] N. Zhang, B. Morgan, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma. Kilovolt AlGaN/GaN HEMTs as switching devices. *Phys. Status Solidi A*, 188(1):213–17, 2001.

[10] M. A. Khan, J. N. Kuznia, J. M. Van Hove, N. Pan, and J. Carter. Observation of a two-dimensional electron gas in low pressure metalorganic chemical vapor deposited GaN-AlGaN heterojunctions. *Appl. Phys. Lett.*, 60(24):3027–9, 1992.

[11] M. A. Khan, J. N. Kuznia, A. R. Bhattarai, and D. T. Olson. Metal semiconductor field effect transistor based on single crystal GaN. *Appl. Phys. Lett.*, 62(15):1786–7, 1993.

[12] S. C. Binari, L. B. Rowland, W. Kruppa, G. Kelner, K. Doverspike, and D. K. Gaskill. Microwave performance of GaN MESFETs. *Electronics Letters*, 30(15):1248–9, 1994.

[13] M. A. Khan, J. N. Kuznia, D. T. Olson, W. J. Schaff, J. W. Burm, and M. S. Shur. Microwave performance of a 0.25 μm gate AlGaN/GaN heterostructure field effect transistor. *Appl. Phys. Lett.*, 65(9):1121–3, 1994.

[14] Y. F. Wu, B. P. Keller, S. Keller, D. Kapolnek, S. P. Denbaars, and U. K. Mishra. Measured microwave power performance of AlGaN/GaN MODFET. *IEEE Electron Device Lett.*, 17(9):455–7, 1996.

[15] M. A. Khan, Q. Chen, M. S. Shur, B. T. Dermott, J. A. Higgins, J. Burm, W. J. Schaff, and L. F. Eastman. CW operation of short-channel GaN/AlGaN doped channel heterostructure field effect transistors at 10 GHz and 15 GHz. *IEEE Electron Device Lett.*, 17(12):584–5, 1996.

[16] Cree achieves major advance in gallium nitride transistor power density. Press release, Durham, NC, December 15, 2003.

[17] L. S. McCarthy, P. Kozodoy, M. J. W. Rodwell, S. P. DenBaars, and U. K. Mishra. AlGaN/GaN heterojunction bipolar transistor. *IEEE Electron Device Letters*, 20(6):277–9, 1999.

[18] S. Yoshida and J. Suzuki. High-temperature reliability of GaN metal semiconductor field-effect transistor and bipolar junction transistor. *Journal of Applied Physics*, 85(11):7931–4, 1999.

[19] J. B. Limb, L. McCarthy, P. Kozodoy, H. Xing, J. Ibbetson, Y. Smorchkova, S. P. DenBaars, and U. K. Mishra. AlGaN/GaN HBTs using regrown emitter. *Electronics Letters*, 35(19):1671–3, 1999.

[20] H. Xing, D. S. Green, L. McCarthy, I. P. Smorchkova, P. Chavarkar, P. Mates, S. Keller, S. DenBaars, J. Speck, and U. K. Mishra. Progress in Gallium Nitride-based Transistors. *Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting*, pages 125–30, 2001.

[21] J. J. Huang, M. Hattendorf, M. Feng, D. J. H. Lambert, B. S. Shelton, M. M. Wong, U. Chowdhury, T. G. Zhu, H. K. Kwon, and R. D. Dupuis. Temperature dependent common emitter current gain and collector-emitter offset voltage study in AlGaN/GaN heterojunction bipolar transistors. *IEEE Electron Device Letters*, 22(4):157–9, 2001.

[22] I. Ben-Yaacov, Y.-K. Seck, and U. K. Mishra. The First AlGaN/GaN CAVETs. *Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD)*, 2002.

[23] Y. Gao, A. R. Stonas, I. Ben-Yaacov, U. K. Mishra, S. P. DenBaars, and E. L. Hu. AlGaN/GaN current aperture vertical electron transistors fabricated by photoelectrochemical wet etching. *Electronics Letters*, 39(1):148–9, 2003.

[24] I. Ben-Yaacov, Y.-K. Seck, S. Heikman, S. P. DenBaars, and U. K. Mishra. AlGaN/GaN Current Aperture Vertical Electron Transistors. *60th Annual Device Research Conference Digest*, pages 31–2, 2002.

[25] I. Ben-Yaacov, Y.-K. Seck, U. K. Mishra, and S. P. DenBaars. AlGaN/GaN current aperture vertical electron transistors with regrown channels. *Journal of Applied Physics*, 95(5), 2004.

2

Modeling, design, and fabrication of AlGaN/GaN CAVETs

2.1 Introduction

PRIOR to this work, CAVET structures had never been fabricated within the III-nitride material system. It was therefore necessary to not only grow the material and process devices but also to develop a theoretical device model and to identify the critical design parameters that affect device performance. Many of the growth and processing requirements for the CAVET were similar to those of AlGaN/GaN HEMTs, so for those steps, the standard HEMT process developed at UCSB was used. However, unlike the GaN HEMT, the CAVET structure cannot be grown completely in one step and then processed. In order to achieve a conducting aperture region with insulating material on ei-

ther side, a regrowth must be performed after some of the initial processing steps. A number of growth and processing techniques therefore had to be developed for use in the fabrication of the CAVET. This chapter describes in detail the theoretical modeling, key design parameters, and growth and processing of AlGaN/GaN CAVETs.

Theoretical modeling of the AlGaN/GaN CAVET was performed by Yee-Kwang Seck using ATLAS, a commercially available device simulator. In this chapter, a summary of the simulation results as well as a qualitative explanation of the basic principles of operation of a CAVET are presented. Additional details of the theoretical analysis can be found in Yee-Kwang Seck's master's thesis [1].

All material was grown by Metal-Organic Chemical Vapor Deposition (MOCVD) using a comercially available Thomas Swan, Ltd. close-spaced vertical reactor. Device processing was performed in the UCSB co-search cleanroom. Facilities used included, among others, an RTS inc. modified GCA I-line wafer stepper, a DC/RF sputtering system by Sputtered Films, Inc., a Temescal e-beam evaporator, PlasmaTherm RIE and PECVD tools, and an AET rapid thermal annealer.

This chapter is arranged into three parts. In the first part, theoretical modeling

and device design are discussed. The second part covers the material growth and characterization. The final part describes all of the device processing involved in the fabrication of AlGaN/GaN CAVETs.

2.2 Principles of operation & theoretical modeling

In a CAVET the intrinsic current flow occurs in two dimensions; electrons first flow horizontally through the 2DEG and then move vertically through the aperture region. This is quite different from the HEMT or the bipolar transistor, where current flow is confined to one dimension. It is therefore critical to develop an accurate model in order to identify which parameters primarily determine the device characteristics. In this section, a qualitative description of the operation of a CAVET is given, followed by a more rigorous theoretical analysis.

Figure 2.1 qualitatively illustrates the fundamental properties of current flow in a CAVET. Current first travels horizontally through the 2DEG, until it reaches the gate. The gate only modulates the current in the 2DEG, so pinch-off occurs in the horizontal direction inside the 2DEG underneath the gate, just like in a standard FET. Electrons which pass the pinch-off point in the channel continue

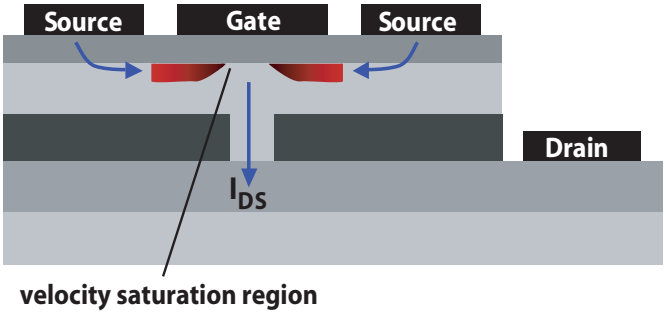

Figure 2.1: Qualitative illustration of current flow in a CAVET. Current first travels through the 2DEG and then pinches off horizontally beneath the gate. Beyond the point of pinch-off, electrons continue to travel horizontally at their saturated velocity v_{sat}, then travel downward through the aperture and continue on to the drain.

---

to travel horizontally at their saturated velocity v_{sat} until they arrive at the aperture, travel downward through the aperture, and are collected at the drain. It is critical that the conductivity of the material inside the aperture as well as in the drain region be much larger than that of the 2DEG so that the entire voltage drop between the source and drain occurs in the 2DEG. This condition ensures that the total current passing through the device is entirely determined by the conductivity of the 2DEG. If this condition is not met, then a significant amount of the applied source-drain voltage is supported across the aperture. In this case, until V_{DS} is very large, the 2DEG does not pinch off and the current does not reach

its saturation value. This is analagous to quasi-saturation in a bipolar transistor, which can occur at large injection currents when the ohmic drop $I_C R_C$ across the collector drift region becomes comparable to the total base-collector voltage V_{CB} [2]. In addition, the conductivity of the 2DEG must be much higher than that of the adjacent bulk GaN directly below the 2DEG to ensure current flow through the 2DEG rather than through the bulk GaN.

The qualitative analysis given here was verified by theoretical modeling of the device. Figure 2.2 compares the electric field distribution as well as the I–V characteristics of an ideal CAVET to one in which the aperture region was more resistive than the 2DEG channel. In the ideal CAVET, illustrated in Figure 2.2(a), pinch-off occurs horizontally in the region above the aperture. In the corresponding I–V curves, the currents saturate nicely, and the magnitude of the currents could be predictably controlled by varying the mobility μ_n and sheet charge n_s in the 2DEG, indicating that the I–V characteristics are entirely determined by the properties of the 2DEG. For the device in which the aperture region was not conductive enough, illustrated in Figure 2.2(b), a significant percentage of the voltage drop occurs across the aperture region. The corresponding currents are much lower than in the ideal device and do not fully saturate at low

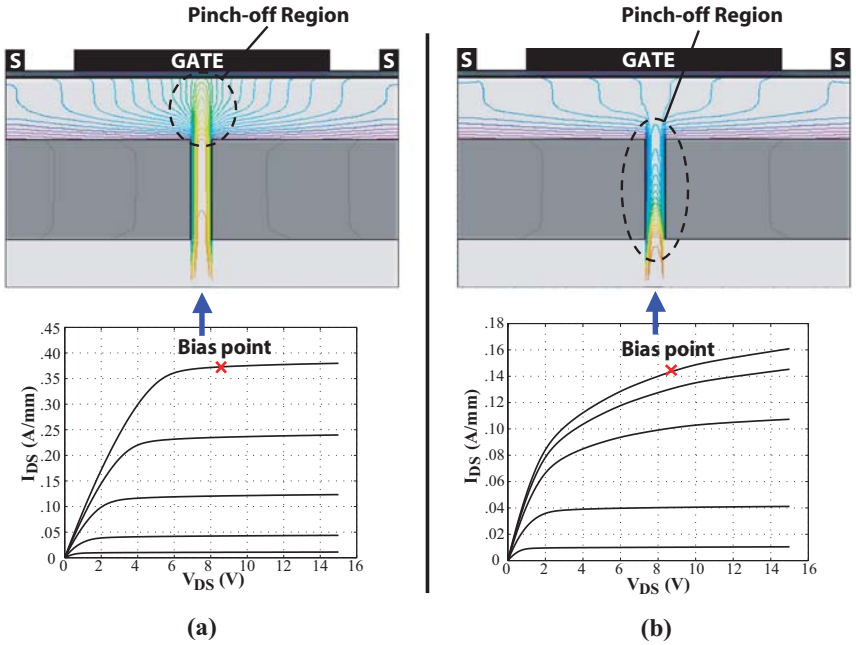

Figure 2.2: Simulation cross section of AlGaN/GaN CAVETs, illustrating constant voltage contour lines and indicating where pinch-off occurs. The two diagrams illustrated correspond to (a) an ideal device and (b) a device in which the aperture region had a very low conductivity. Also pictured are the corresponding simulated I–V characteristics for each device.

---

values of V_{DS}, indicative of the quasi-saturation effects that are present in this device. In addition, the current changes very little when the 2DEG properties are varied, indicating that the I–V characteristics are dominated by the electrical charateristics of the aperture region.

It should also be noted that in both cases, the high field region, corresponding

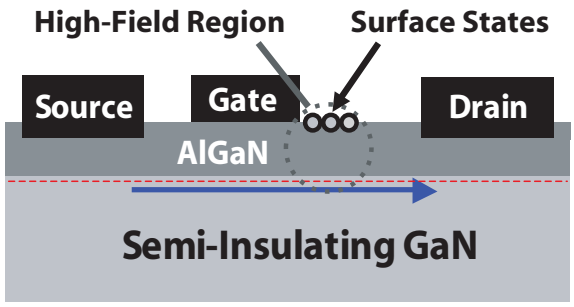

Figure 2.3: Schematic diagram of where the high field region occurs in a GaN-based HEMT.

---

to the region where pinch-off occurs, is buried in the bulk below the gate. This sort of field distribution is fundamentally different from that of a HEMT. In a HEMT, the high field region is located at the AlGaN surface on the drain-side edge of the gate, as illustrated schematically in Figure 2.3. The high surface fields in AlGaN/GaN HEMTs lead to the charging of AlGaN surface states, resulting in the DC-RF dispersion which is commonly observed [3]. In a CAVET, because the high field region is buried in the bulk, DC-RF dispersion should be mitigated. A more detailed analysis of DC-RF dispersion is presented in § 3.6.

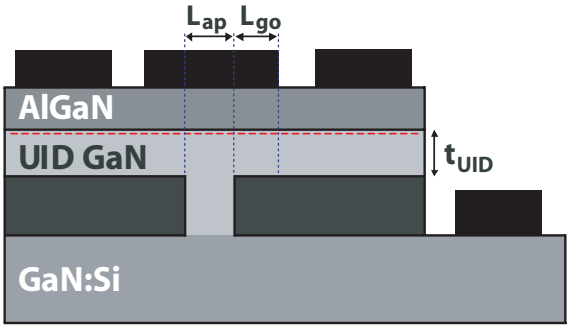

Figure 2.4: Schematic diagram of an AlGaN/GaN CAVET indicating critical design parameters.

2.3 Design parameters

In designing an optimal CAVET structure, a number of design parameters and their effects on both DC and RF device characteristics need to be considered. Some of the more critical parameters include the aperture length L_{ap}, the doping in the aperture region N_{ap}, the gate-overlap length L_{go}, and the thickness of the UID GaN directly below the AlGaN t_{UID}. These parameters are indicated in the diagram in Figure 2.4. The resistance of the aperture region is determined both by the resistivity of the material inside the aperture and by L_{ap}. The resistivity of the material in the aperture region is inversely proportional to N_{ap}, so L_{ap} and N_{ap} are therefore coupled with respect to the resistance of the aperture region,

and so they must be optimized simultaneously. In order to ensure that the resistance of the aperture region is extremely low, it is important to make sure that the L_{ap}·N_{ap} product is not too small. However, increasing N_{ap} raises the peak electric field in the device, resulting in a decrease in the breakdown voltage V_{BR}. Additionally, making L_{ap} too large increases the gate-drain capacitance C_{gd}, potentially resulting in a decline in RF performance (see Chapter 6). In this study, for devices with $\mathrm{N}_{ap} \approx 4{\times}10^{17}$, the optimal aperture length was found to be $\sim$ 1–2 μm.

The gate overlap length primarily determines the gate-source capacitance C_{gs} in a CAVET. Because the current-gain cutoff frequency f_τ is predominantly limited by C_{gs}, it is important to keep L_{go} as small as possible. This is analogous to reducing the gate length of a normal HEMT. However, making L_{go} too small can result in source leakage underneath the 2DEG at higher values of V_{DS} (a complete analysis of leakage currents is presented in Chapter 4). The thickness of the UID GaN layer t_{UID} also affects leakage underneath the 2DEG. By making t_{UID} too large, the UID GaN is not fully depleted, resulting in electron flow beneath the 2DEG. However, making t_{UID} smaller also brings the 2DEG closer to the insulating layer, which was found to reduce the μ_n·n_s product in the 2DEG.

2.4 Device layout

A number of different device layouts are possible for a CAVET. The ideal layout would be to have the drain metal physically located below the aperture on the back side of the wafer. This requires using a conducting substrate, such as n-type SiC. However, performing RF testing on a device requires ground-signal-ground (GSG) probe pads, which are much more difficult to implement when the drain is on the back side. In this study, two different coplanar waveguide (CPW) structures were employed. These two layouts are illustrated in Figure 2.5. Two-sided CAVETs, illustrated in Figure 2.5(a), had gate widths $W_{gate} = 50$ μm, corresponding to a total source width $W_{source} = 2{\cdot}W_{gate} = 100$ μm. One-sided CAVETs, shown in Figure 2.5(b), had gate widths $W_{gate} = W_{source} = 150$ μm. The two-sided devices had sources on either side of the aperture, as would normally be desired. However, even though the gate widths of these devices were somewhat smaller than those of the one-sided CAVETs, current crowding was still a problem, since the drain metal was located at the far end of the aperture. The current flowing through the portion of the aperture furthest from the gate was less than that flowing through the rest of the aperture. As a result, the measured

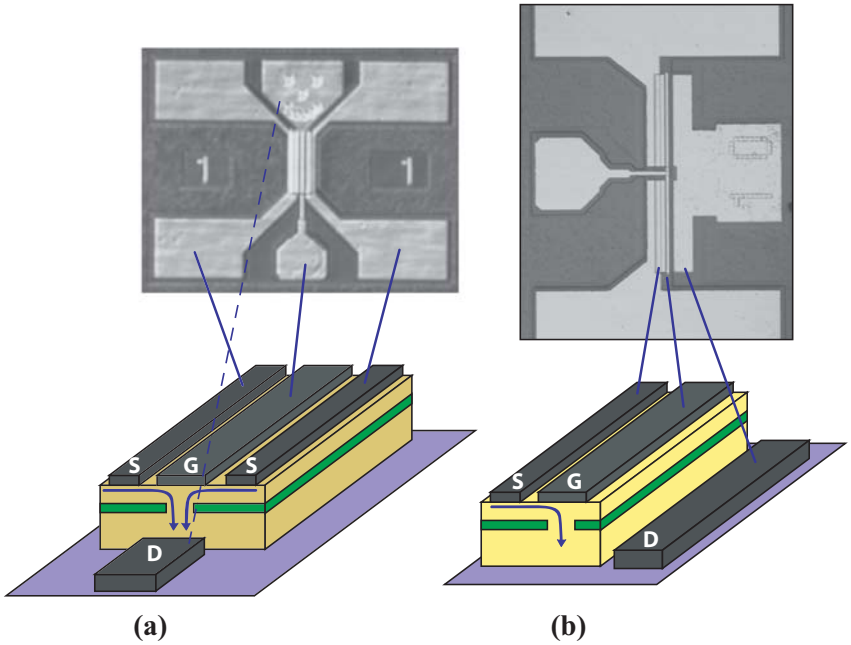

Figure 2.5: Schematic diagrams of the two device layouts used in this work, along with optical photographs of fabricated devices.

---

current densities and transconductances were a bit lower than their expected values for these devices. The devices in Figure 2.5(b) were therefore much more useful in analyzing intrinsic device properties.

Layer	Thickness [nm]	Temp [°C]	Press [Torr]	NH_3 [lpm]	TMGa [sccm]	Si, Fe, or Mg [sccm]
LT GaN	~ 100	624	760	6	60.0	N/A
GaN	600	1160	760	6	67.5	N/A
GaN:Si	1800	1160	760	6	67.5	0.6
GaN:(Fe/Mg)	400	1160/1130	760	6	67.5	26/205

Table 2.1: Sample growth conditions for CAVET base structure grown in a Thomas Swan close-spaced vertical MOCVD reactor.

2.5 Material growth issues

All material in this work was grown by MOCVD on c-plane sapphire substrates, resulting in wurtzite GaN grown in the $<0001>$ direction. The material growth involved in the fabrication of a CAVET consists of two parts. First, an initial base structure is grown. The base structure consists of a thick n-type drain layer followed by a layer of Fe- or Mg-doped GaN, which acts as an insulating layer [see Figure 2.6(a)]. A sample of the growth conditions for the base layers is given in Table 2.1. After the base structure is grown, the wafer must be removed from the MOCVD reactor so that an aperture region can be etched through the insulating layer. The second part of the growth involves a maskless MOCVD regrowth. The wafer is reinserted into the MOCVD reactor, and the material

inside the aperture region as well as the UID GaN layer and the AlGaN cap are all grown.

2.5.1 Designing the insulating layer

One of the most important considerations in fabricating a CAVET is what material to use for the insulating layer. One possible candidate is to deposit an insulator, such as SiO_2, and perform a lateral epitaxial overgrowth (LEO) [4]. However, regrowth in the presence of an insulator which contains either silicon or oxygen often results in unintentional doping of the regrown material, thus making it difficult to control the electronic properties of the regrown material. In addition, even if an insulator is used which does not lead to unintentional doping, such as AlN, the growth conditions required to achieve lateral overgrowth do not typically lead to material best suited for electronics applications. Also, it is very difficult to achieve lateral growth rates which are much higher than the vertical growth rate without compromising material quality even further, and so the resulting wing region would have to be very narrow. After accounting for the necessary gate overlap length and source-gate spacing, there would be little or

no material left at the end of the overgrown wings for the source ohmic contacts. Another option, which has been successful in the fabrication of CAVETs, is to use a photoelectrochemical (PEC) wet etch to undercut the source region, resulting in an insulating region that consists of air [5]. The approach that was initially pursued in this work was to incorporate a dopant into the GaN in the insulating layer, resulting in insulating GaN. The two dopants tested were Fe and Mg, and devices were successfully fabricated using each of these. In subsequent devices, an aluminum ion implantation was used to render the GaN insulating. The ion implantation technique will be discussed in detail in Chapter 5.

2.5.2 MOCVD regrowth

Figure 2.6 gives a step-by-step description of the entire regrowth. After the aperture region is etched away, the initial structure is reinserted into the MOCVD reactor for regrowth. The sample is first heated up in nitrogen and NH_3 to the regrowth temperature of 1160 °C. Interrupted growth studies verified that even before TMGa is introduced into the reactor, the aperture partially fills with GaN as a result of mass transport of material from the surface into the aperture [6, 7],

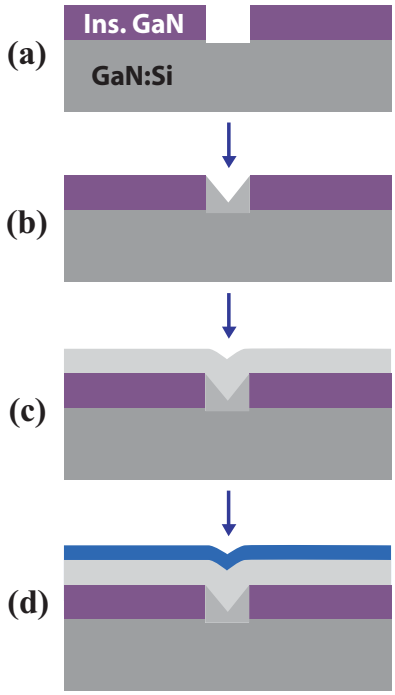

Figure 2.6: Diagram depicting MOCVD regrowth. (a) Initial structure is etched and reinserted into MOCVD reactor. (b) As sample is heated to regrowth temperature, aperture partially fills with GaN. (c) UID GaN is grown. (d) AlGaN is grown, surface not completely planar.

---

as indicated in Figure 2.6(b). For this to occur, gallium is provided by the desorption of GaN from the surface of material near the aperture, and nitrogen is provided by the NH_3. Once the regrowth temperature has been reached, TMGa is injected into the reactor, and the UID GaN layer is grown, followed by the AlGaN cap, as illustrated in Figure 2.6(c-d). The entire regrowth is performed

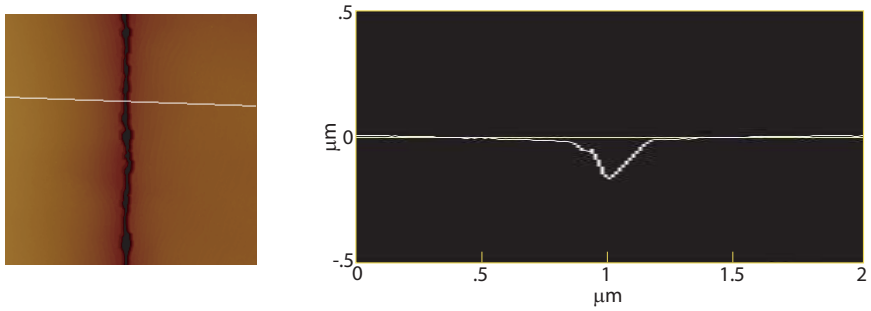

Figure 2.7: (a) 7×7 μm AFM image and (b) cross section analysis of surface directly above the aperture after regrowth.

---

with nitrogen as the carrier gas in order to prevent Mg in the insulating layer from being passivated by hydrogen [8]. The surface directly above the apertures does not entirely planarize during the regrowth; a small depression can still be observed, as seen in the AFM image of the surface after regrowth in Figure 2.7. Material inside and above the aperture region therefore is not grown on the c-plane, but rather on an inclined or vertical facet.

If the surface above the aperture region has a very steep indentation and the gate metal is placed directly on top, large peaks in the electric field near the indentation could potentially occur when the device is under bias. It is therefore important that the regrown surface directly above the aperture be as planar

as possible. The most important parameter in determining how well the surface planarizes is the regrowth temperature, although the V/III ratio also plays a smaller role. In general, higher growth temperatures and lower V/III ratios tend to favor planarization. In addition, it was found that nonoptimal regrowth conditions can result in large leakage currents. A discussion of regrowth optimization for the elimination of leakage currents is given in Chapter 4.

2.5.3 Growth of AlGaN/GaN heterostructures

The final step in the material growth involves growing a thin AlGaN layer on top of UID GaN to form the 2DEG which supplies the current in the device. The primary requirement for the 2DEG in both CAVETs and HEMTs is that it have a large $\mu_n \cdot n_s$ product. The AlGaN growth process for HEMTs had already been fully developed at UCSB, so identical conditions were used for the AlGaN growth in the CAVET. The Al composition in all devices was between 30% and 35%. Additionally, in all devices other than the first ones fabricated, a thin AlN layer was placed between the AlGaN and the adjacent UID GaN, thereby increasing the $\mu_n \cdot n_s$ product in the 2DEG by increasing the effective ΔE_C and

decreasing alloy scattering from the AlGaN [9]. This AlN layer is also part of the standard UCSB HEMT structure.

2.6 Device processing

The following section gives a detailed description of the entire fabrication process of a CAVET, describing all of the device processing and providing the details of the material growth. In devices which contained an ion-implanted insulating layer, the process had to be varied slightly. Those revisions will be described in Chapter 5.

Fabrication began with the growth of the initial base structure, which consisted of a 2 μm n-type (Si doped) GaN drain layer followed by a 0.4 μm insulating GaN layer [see Figure 2.8(a)]. Next, channel apertures were etched through the insulating GaN by Cl_2 reactive ion etching (RIE), as illustrated in Figure 2.8(b). Aperture widths (L_{ap}) ranged from 0.6 μm to 3 μm, and gate overlap lengths (L_{go}) ranged from 0.3 μm to 5 μm. Alignment marks on each die were then covered by sputtering AlN so that the marks would be visible following regrowth. The wafer was then placed back into the MOCVD chamber and a maskless re-

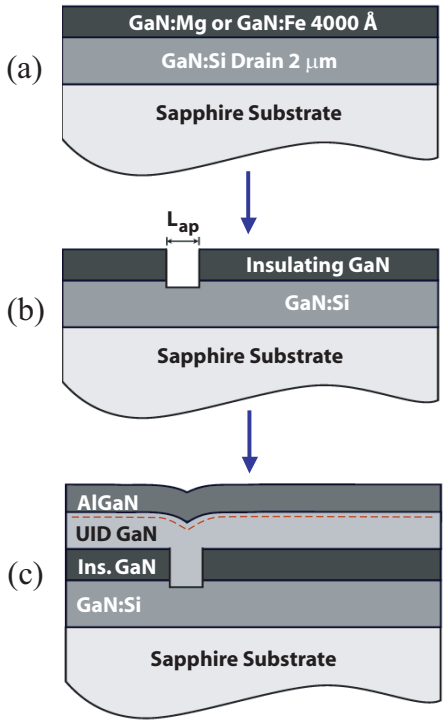

Figure 2.8: Initial growth and regrowth for AlGaN/GaN CAVETs.

---

growth was performed. 1700-2500 Å of UID GaN was grown, followed by a 250 Å AlGaN cap, resulting in the structure shown in Figure 2.8(c). A two-dimensional electron gas (2DEG) is present in the GaN near the AlGaN/GaN heterointerface, enabling the formation of ohmic source contacts and providing the charge that is collected at the drain.

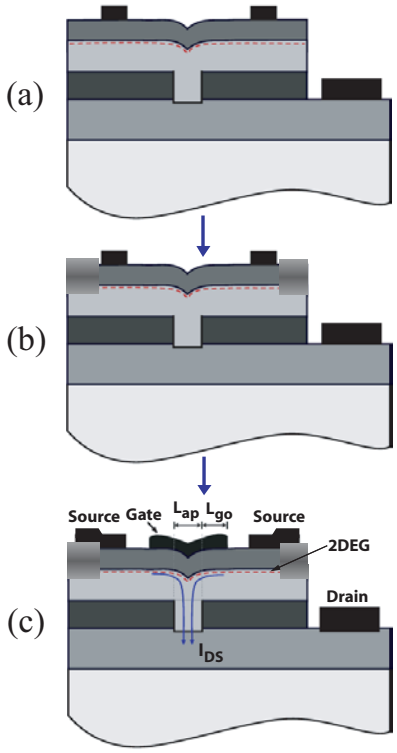

Figure 2.9: Process flow for AlGaN/GaN CAVETs.

Next, a device mesa for the source and gate region was formed with Cl_2 RIE, and Ti/Al/Ni/Au (200/1500/375/500 Å) were evaporated and annealed at 870 °C for 30 seconds to form ohmic source and drain contacts [see Figure 2.9(a)]. The source metal contacts the 2DEG near the AlGaN/GaN heterointerface, while the drain metal contacts the Si-doped GaN layer at the base of the structure. After

this, the area on the device mesa where the source and gate probe pads sit was isolated from the source region to reduce leakage currents as well as extrinsic parasitics. A 600 Å Cl_2 RIE etch was performed to remove the AlGaN and some of the underlying GaN from this area, followed by a 2500 Å electron beam SiO_2 depostion, as illustrated in Figure 2.9(b). Next, 300/3500 Å of Ni/Au was evaporated for a gate metallization. Finally, Ti/Au (300/3000 Å) was evaporated for source and gate probe pads, resulting in the device illustrated in Figure 2.9(c). None of the devices with Mg- or Fe-doped insulating layers contained any kind of surface passivation layer. In the devices with ion implanted insulating layers, devices were passivated with SiN and retested after all DC and RF testing had been performed.

2.7 Summary

Device design and modeling, as well as growth and fabrication procedures, were all introduced. A theoretical model was developed which accurately described operation of an ideal device as well one in which the aperture region was not adequately conductive. Key design parameters, including the aperture length

L_{ap}, the gate overlap length L_{go}, the n-type doping level in the aperture region N_{ap}, and the UID layer thickness t_{UID}, were identified and discussed. Two different device layouts were described, and the merits of each layout were presented. Various growth issues, such as regrowth on a non-planar surface and formation of AlGaN/GaN heterostructures, were addressed. The foundation for the device processing used in this work was presented, and a step-by-step description of the entire fabrication procedure was given.

References

[1] Yee-Kwang Seck. Masters thesis, University of California, Santa Barbara, in preparation.

[2] David J. Roulston. *Bipolar Semiconductor Devices*. New York: McGraw-Hill, Inc., 1990, pp. 259-64.

[3] Robert Coffie. *Characterizing and Suppressing DC-to-RF Dispersion in AlGaN/GaN High Electron Mobility Transistors*. PhD thesis, University of California, Santa Barbara, 2003.

[4] Paul T. Fini. *Threading dislocation reduction in gallium nitride thin films on sapphire via lateral epitaxial overgrowth*. PhD thesis, University of California, Santa Barbara, 2001.

[5] Y. Gao, A. R. Stonas, I. Ben-Yaacov, U. K. Mishra, S. P. DenBaars, and E. L. Hu. AlGaN/GaN current aperture vertical electron transistors fabricated by photoelectrochemical wet etching. *Electronics Letters*, 39(1):148–9, 2003.

[6] S. Nitta, M. Kariya, T. Kashima, S. Yamaguchi, H. Amano, and I. Akasaki. Mass transport and the reduction of threading dislocation in GaN. *Appl. Surf. Sci.*, 159:421–6, 2000.

[7] S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra. Mass transport regrowth of GaN for ohmic contacts to AlGaN/GaN. *Appl. Phys. Lett.*, 78(19):2876–8, 2001.

[8] Peter Kozodoy. *Magnesium-doped gallium nitride for electronic and opto-electronic device applications*. PhD thesis, University of California, Santa Barbara, 1999.

[9] L. Shen, S. Heikman, B. Moran, R. Coffie, N.-Q. Zhang, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra. AlGaN/AlN/GaN high-power microwave HEMT. *IEEE Elec. Dev. Lett.*, 22(10):457–9, 2001.

3

AlGaN/GaN CAVETs with regrown aperture regions

3.1 Introduction

CURRENT aperture vertical electron transistors present a number of processing and material challenges distinct from other electronic devices in the III-Nitride material system, some of which were discussed in Chapter 2. Maintaining a high $\mu_n \cdot n_s$ product in the 2DEG is considerably more difficult than in a HEMT, since the source region sits on top of a Mg-doped or Fe-doped layer and must be regrown. Design and fabrication of the aperture region must be optimized to ensure that it is highly conductive. Additionally, because the drain region is located directly below the source and gate regions, leakage currents are very difficult to suppress.

This chapter introduces the initial results for devices with both Fe-doped and Mg-doped insulating layers. In the first devices, currents were much lower than expected, and for the devices with Mg-doped insulating layers, the currents never saturated. Improvements in device design as well as processing led to devices with much higher currents and negligible DC-RF dispersion. A complete analysis of dispersion was conducted, and it was shown conclusively that the dispersion prevalent in AlGaN/GaN HEMTs is indeed surface related, and that since there is no surface on the drain side of the gate in the CAVET geometry, DC-RF dispersion is mitigated.

3.2 Initial Results

3.2.1 First demonstration of an AlGaN/GaN CAVET

In October 2001, the first GaN-based CAVETs were demonstrated at UCSB. Devices with both Fe-doped and Mg-doped insulating layers were fabricated concurrently. After fabrication, electronic device characterization was performed using a Tektronix 370A programmable curve tracer. Both DC and pulsed I–V

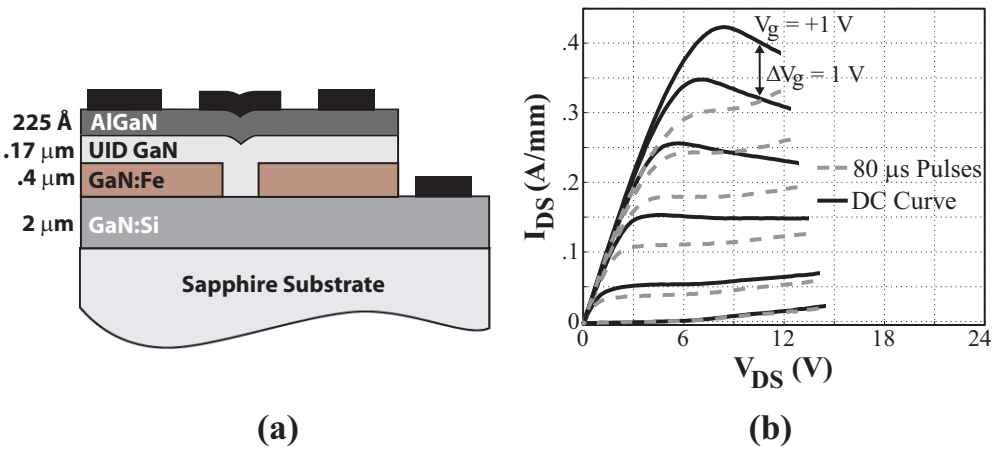

Figure 3.1: (a) Device schematic and (b) I–V characteristics for a two-sided CAVET with an Fe-doped insulating layer. For this device, the Al composition in the AlGaN $x_{Al} = 35\%$, the Si doping level in the drain region was $\sim 1\times10^{18}$, the Fe doping level in the insulating layer was $\sim 1\times10^{19}$, $L_{ap} = 0.6$ μm, and $L_{go} = 2$ μm.

characteristics were obtained.

3.2.2 Devices with Fe-doped insulating layers

A device schematic along with the DC I_{ds}–V_{ds} characteristics of a two-sided CAVET with an Fe-doped insulating layer are illustrated in Figure 3.1. This device had a maximum source-drain current I_{max} of 430 mA/mm, a pinch-off voltage V_p of – 4 V, and an extrinsic transconductance g_m of $\sim$ 100 mS/mm

at $I_{ds} \sim 350$ mA/mm and $V_{ds} \sim 9$ V. The current in this device was relatively low compared to that of a HEMT; a HEMT with a similar AlGaN layer would typically have an I_{max} of around 1 A/mm. However, the current does saturate, and qualitatively, the I–V charateristics resemble the ideal predicted curves that were illustrated in Figure 2.2(a). Additionally, device DC characteristics were found to be independent of the aperture length L_{ap} for aperture lengths ranging from 0.6 μm to 2 μm, indicating that the maximum current I_{max} in these devices is determined by the available charge in the 2DEG and not by the conductivity of the aperture region. These observations led us to conclude that although the aperture region had a sufficiently low resistance, the conductivity of the 2DEG was somehow lower than expected. The low currents in these devices were eventually determined to result from Fe incorporating into the regrown material directly above the insulating layer. The details of how this occurred are presented in §3.3.

Relatively large parasitic leakage currents, which are evident in Figure 3.1(b), prevented a meaningful measure of the breakdown voltage. A complete analysis of leakage currents is presented in Chapter 4. A comparison of the DC device characteristics to those where the gate was pulsed from pinchoff to their final

value reveals that these devices do exhibit some dispersion for an 80 μs pulse width. This dispersion was thought to be related to traps in the Fe-doped layer and not to any surface effects. It should be noted that all current densities (I_{ds}) and transconductances (g_m) reported in this dissertation are per source pad, so that a meaningful comparison to HEMTs can be made (recall that $W_{source} = 2 \cdot W_{gate}$, since there are two source pads).

3.2.3 Devices with Mg-doped insulating layers

Figure 3.2 shows a device schematic along with the DC I_{ds}–V_{ds} characteristics of a two-sided CAVET with a Mg-doped insulating layer. In this device, the currents were extremely low, even as compared to CAVETs with Fe-doped insulating layers, and the currents never saturated. Device I–V characteristics were qualitatively similar to the non-ideal predicted curves in Figure 2.2(b). Additionally, currents measured in these devices were dependent on L_{ap}; devices with smaller apertures had smaller currents, indicating that the current was being limited by the low conductivity of the aperture region. As will be discussed in §3.3, the low conductivity of the aperture region was found to result from Mg

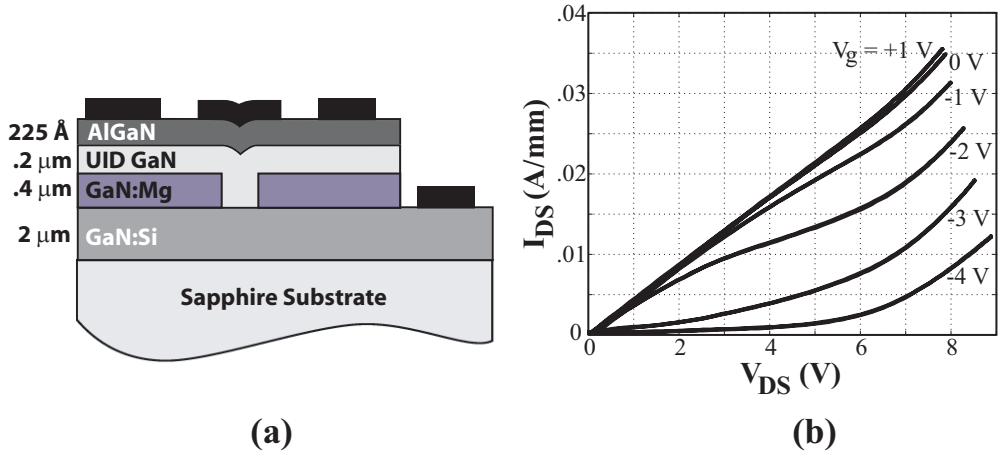

Figure 3.2: (a) Device schematic and (b) I–V characteristics for a CAVET with a Mg-doped insulating layer. For this device, the Al composition in the AlGaN $x_{Al} = 35\%$, the Si doping level in the drain region was $\sim 1\times10^{18}$, the Mg doping level in the insulating layer was $\sim 1\times10^{19}$, $L_{ap} = 2$ μm, and $L_{go} = 2$ μm.

incorporating into all of the regrown material.

3.3 Regrowth on Fe-doped and Mg-doped GaN

Although currents were low in devices with both Fe-doped and Mg-doped insulating layers, the mechanism for current reduction appeared to be fundamentally different for each of these devices. In devices with an Fe-doped layer, although the 2DEG was not as conductive as expected, the aperture region was

sufficiently conductive. In contrast, for devices with Mg-doped layers, the aperture region was also overly resistive. The current reduction in both devices was determined to result from Fe or Mg being unintentionally incorporated into the regrown material during the regrowth. However, the mode by which each dopant was incorporated into the regrown material was fundamentally different, which is why the I–V characteristics of the two sets of devices were so dissimilar.

When material is regrown directly on top of Mg-doped or Fe-doped GaN, proper surface treatment must be performed to ensure that no Mg or Fe is incoroporated into the regrown material. When GaN is doped with Fe, studies have shown that once the Fe is shut off during growth, an Fe-rich layer is still present at the surface [1]. When additional material is grown on top, the Fe tends to ride along the surface and is consequently incorporated into the regrown material. In order to remove the Fe from the surface, it is necessary to remove the wafer from the reactor and perform an acid etch. Dipping the sample in H_2SO_4, HNO_3, H_3PO_4, HCl, and HF for five minutes each [1] removes the excess Fe from the surface, and any material which is subsequently grown on top contains no unintentional Fe doping.

In the fabrication of a CAVET, the initial growth step ends after the insulating

layer has been grown, so when the wafer is removed from the reactor, the first step performed should be the forementioned acid treatment. Since this treatment was not performed for the device in Figure 3.1, Fe which remained on the surface continued to propagate upwards along the surface during regrowth, thus incorporating into all of the material directly above the insulating layer. As a result, the conductivity of the 2DEG was reduced. However, the Fe did not appear to re-enter the vapor phase, since the aperture region was sufficiently conductive. Had the Fe re-enterred the vapor phase, the material in the aperture region would have also been unintentionally Fe-doped, and so device I–V curves would have more closely resembled the non-ideal characteristics illustrated in Figure 2.2(b).

When growth of Mg-doped GaN is terminated, a Mg-rich layer is also present at the surface, which causes Mg to incorporate into any material that is subsequently regrown on top [2]. However, unlike Fe, Mg which remains on the surface does re-enter the vapor phase during regrowth and thus incorporates into all of the regrown material. In the case of the regrowth performed for the CAVET in Figure 3.2, this meant that Mg was incorporated into all of the regrown material, including the GaN in the aperture region, which resulted in a highly resistive aperture region. As a result, the I–V characteristics of this device were qualita-

tively very similar to the non-ideal predicted curves illustrated in Figure 2.2(b). Fortunately, this excess Mg can be removed by dipping the sample for two minutes in buffered HF and two minutes in HCl [2] prior to regrowth.

Previously, Xing *et al.* had reported Mg being incorporated into n-type GaN regrown on a Mg-doped GaN layer and had attributed the accumulation of Mg at the surface to the commonly seen Mg memory effect in MOCVD [2]. However, their experiments did not identify conclusively the mechanism by which the Mg was incorporated into the regrown material. More specifically, from their results it was unclear whether the Mg diffused into the regrown material or re-enterred the vapor phase and was incorporated as such. The studies presented here confirm that the latter of these two possibilities is what actually occurred.

3.4 Insulating layer: Fe vs. Mg doping

In order to evaluate the resistivity of each of the insulating layers, diode structures which resemble a CAVET with no aperture were fabricated, as illustrated in Figure 3.3. For each of the structures, the GaN:Si drain region and the insulating layer were grown initially. The wafers were then removed from the

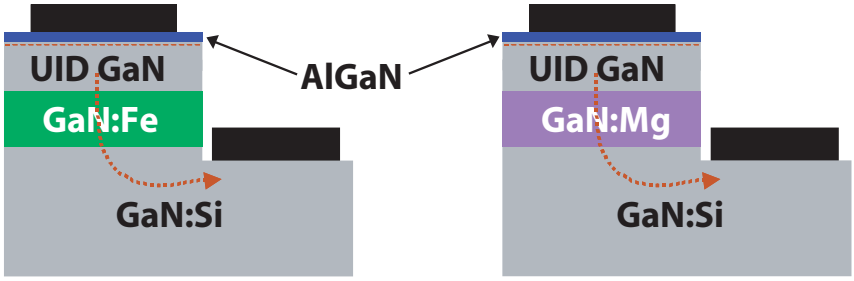

Figure 3.3: Diode structures fabricated to evaluate insulating properties of Fe-doped and Mg-doped insulating layers. In each of the diodes, the insulating layer was 4000 Å thick and contained $\sim 10^{19}$ cm^{-3} Fe or Mg dopant atoms.

MOCVD reactor and dipped in various acids to remove excess Fe or Mg from the surface, as described in §3.3. The two wafers were then placed side by side in the MOCVD reactor, and the UID GaN and AlGaN layers were grown simultaneously on both wafers. In each of the diodes, the insulating layer was 4000 Å thick and contained $\sim 10^{19}$ cm^{-3} Fe or Mg dopant atoms. Finally, I–V characterization of each of the diodes was performed to measure the leakage currents. For the device with an Fe-doped insulating layer, leakage currents as high as 2 A/mm^2 were measured at 14 V bias. In the device with a Mg-doped layer, leakage currents remained below 10 mA/mm^2 for all biases below breakdown. Leakage was clearly much less severe for the Mg-doped insulating layer than for the Fe-doped layer.

In GaN, although the exact energy level associated with Fe doping is uncertain, in two separate studies the $Fe^{3+/2+}$ acceptor level was predicted to be located 2.6 eV [3] and 3.17 eV [4] above the valence band maximum, respectively. The Mg acceptor level in GaN has been experimentally determined to be located 0.17 eV above the valence band maximum [5]. If the Fermi level in the insulating layer is assumed to be located approximately at the Fe or Mg dopant level, then the barrier to electron flow is clearly much larger with a Mg-doped GaN layer than with an Fe-doped layer. It is likely that the large barrier formed with the Mg-doped GaN is responsible for the superior current blocking properties of the Mg-doped layer.

3.5 Improved CAVETs

After fabrication and testing of the initial devices, a number of changes in the device processing were implemented for the second generation of CAVETs. The most important improvement was to implement the surface treatment described in §3.3, which eliminated the unintentional doping in the regrown material. Secondly, a thin ($\sim$ 6 Å) AlN layer was added underneath the AlGaN to increase the

$\mu_n \cdot n_s$ product in the 2DEG. The UID GaN underneath the AlGaN was also made slightly thicker in hopes of increasing the conductivity of the 2DEG. Finally, an n^- subcollector-like drift region was inserted directly below the aperture region which was meant to support some of the applied source-drain voltage, thus increasing the breakdown voltage of the device. The complete device layer structure is illustrated in Figure 3.4(a). Also, because Fe-doped insulating layers were found to have relatively poor current blocking characteristics, and devices with Fe-doped layers exhibited some DC-RF dispersion, only Mg-doped insulating layers were employed in the second generation of devices.

3.5.1 Device results

The device layer structure and DC I_{ds}–V_{ds} characteristics of a second generation CAVET with a Mg-doped insulating layer are illustrated in Figure 3.4. This device had a maximum source-drain current I_{max} of 750 mA/mm, a pinch-off voltage V_p of – 6 V, and an extrinsic transconductance g_m of $\sim$ 120 mS/mm at $I_{ds} \sim$ 650 mA/mm and $V_{ds} \sim$ 7 V. The currents and transconductances in this device were all significantly higher than any that had been previously achieved in

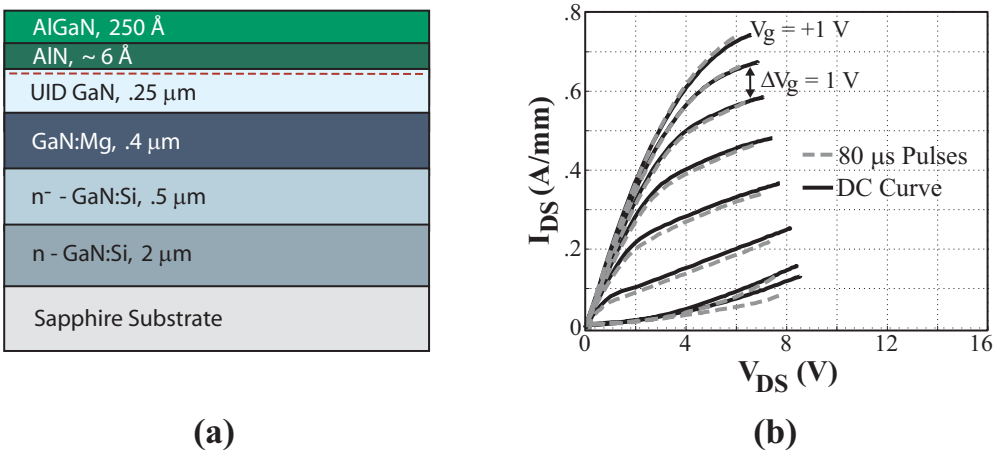

Figure 3.4: (a) Layer structure and (b) I–V characteristics for a second generation CAVET. For this device, the Al composition in the AlGaN $x_{Al} = 33\%$, the Si doping level in the drain region was $\sim 1\times10^{18}$, the Si doping level in the n^- drift region was $\sim 1\times10^{17}$, the Mg doping level in the insulating layer was $\sim 1\times10^{19}$, $L_{ap} = 2$ μm, and $L_{go} = 1$ μm.

AlGaN/GaN CAVETs. Although leakage currents in this device still prevented a meaningful measure of the 3-terminal breakdown voltage, the 2-terminal breakdown voltage was successfully measured and was found to be $\sim$ 65 V, although this value may have also been larger in the absence of gate leakage. A comparison of the DC device characteristics to those where the gate was pulsed from pinchoff to their final value reveals that these devices exhibit almost no dispersion for an 80 μs pulse width. This further confirms the conclusion that the

dispersion observed in devices with an Fe-doped insulating layer was somehow related to traps in that layer. Device DC electronic characteristics were found to be independent of the aperture length L_{ap} for aperture lengths ranging from 0.8 μm to 2 μm, indicating that the acid treatment successfully removed the excess Mg from the surface and prevented unintentional Mg doping of the regrown material. The current in some devices which had an aperture length smaller than 0.8 μm was lower than those with larger apertures, indicating that the current in these devices was being limited by the conductivity of the aperture region. For devices with very small apertures, it is likely that the low conductivity of the aperture region resulted from side-depletion of the aperture, since it is situated between two layers which are highly doped with Mg.

3.5.2 Electrical characterization of the 2DEG

Because the sheet charge and mobility in the 2DEG play such a crucial role in determining device performance, it is important that both be measured. Specifically, it is critical to determine whether the insulating layer, which lies directly underneath the source region, has any effect on μ_n or n_s in the 2DEG. These

parameters are typically characterized by performing Hall measurements using the van der Pauw method [6]. For this study, measurements were performed using a custom built Hall setup consisting of a Kiethley 220 programmable current source, a Hewlett Packard 34401A multimeter, and an electromagnet equipped with a digital teslameter.

For GaN HEMTs, the sample preparation for Hall measurements is quite simple and only takes a few minutes. A square piece of material can be cleaved from the wafer, and ohmic contacts can be placed in each corner by lightly scratching the surface and then placing a small dot of indium metal on top of the scratch and pressing down on it. Because the 2DEG is the only conducting region in the HEMT structure, no special precautions must be taken to prevent parallel conduction.

When performing Hall measurements of the 2DEG in a CAVET structure, it is important to ensure that the ohmic contacts are only contacting the 2DEG and not the n-type drain region below the insulating layer. Otherwise, the measured sheet charge will be the sum of the charge in the 2DEG and that of the drain region, and the measured mobility will be a weighted average of the mobilities of both these regions. To contact the 2DEG, the Hall sample was coated with

photoresist, stepper lithography was performed to expose the contact regions, and Ti/Al/Ni/Au (200/1500/375/500 Å) were evaporated and annealed at 870 °C for 30 seconds to form ohmic contacts.

Hall measurements were performed on a structure similar to the one shown in Figure 3.4(a). The sheet charge n_s of the 2DEG was measured to be $\sim 1.4\times10^{13}$ cm^{-3}, and the mobility μ_n was $\sim$ 900 cm^2/V·s. For a HEMT structure grown under similar conditions with an AlGaN/AlN cap identical to the one in this experiment, n_s was also measured to be $\sim 1.4\times10^{13}$ cm^{-3}, but μ_n was found to be $\sim$ 1450 cm^2/V·s. The reduction in the mobility for the CAVET structure was most likely a result of regrowing on a Mg-doped layer, combined with the close proximity of the Mg-doped layer to the 2DEG. However, the values measured for the CAVET structure were easily adequate for the fabrication of working devices.

3.6 Analysis of DC-RF dispersion

In AlGaN/GaN HEMTs, DC-RF dispersion has been attributed to the charging of surface traps at the AlGaN surface in the gate-drain access region [7],

which were shown schematically in Figure 2.3. When the device is under bias, large electric fields are present at the drain-side edge of the gate, which causes the surface states to fill with electrons until the surface is approximately at the same potential as the gate. When an RF signal is then applied to the gate, the surface states do not respond as quickly as the metallic gate, so the potential at the surface is not able to vary as quickly as the applied RF signal, resulting in the DC-RF dispersion that is commonly observed. A more detailed description of dispersion in AlGaN/GaN HEMTs is given in Robert Coffie's PhD thesis [7].

In a CAVET, the drain region is located beneath the gate. As a result, when the device is under bias, the high field region is buried in the bulk rather than at the surface, as was shown in our simulations in Figure 2.2. The electric field at the surface, which results from the small potential difference between the gate and the source, is relatively small, so the surface states should not fill up with electrons and DC-RF dispersion should be mitigated. The I–V characteristics shown in Figure 3.4 support this hypothesis; the device shows negligible dispersion for 80 μs pulses.

In order to further verify this surface-state model for dispersion, the three structures illustrated in Figure 3.5 were fabricated on the same material and then

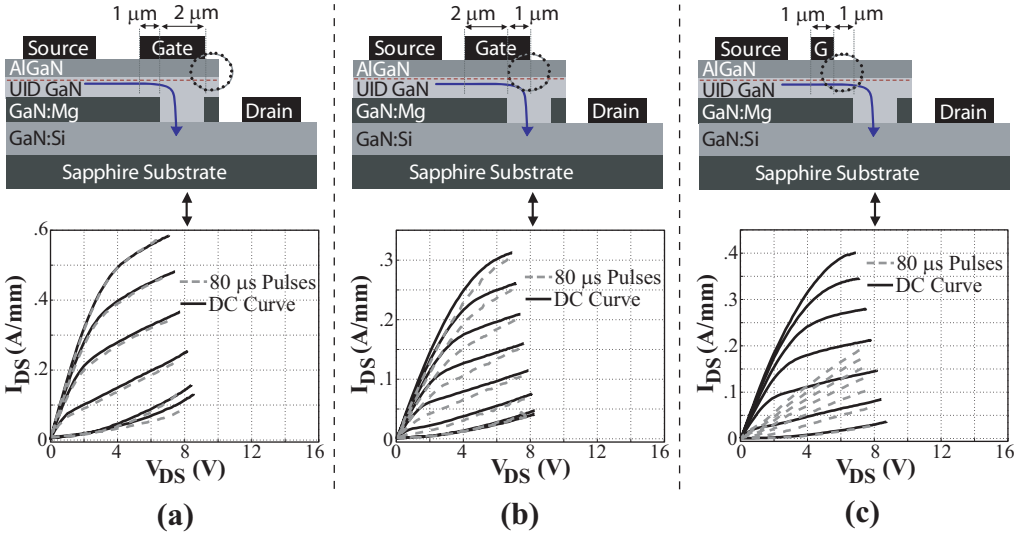

Figure 3.5: Three CAVET structures fabricated in order to verify the surface-state model for DC-RF dispersion, along with corresponding I–V characteristics. (a) Gate completely covers the aperture, drain-side edge of gate is far from the current path, dispersion is negligible. (b) Gate partially covers the aperture, drain-side edge of gate is near the current path, small amount of dispersion is present. (c) Gate is completely offset from the aperture, current passes directly underneath drain-side edge of gate, device exibits a large amount of dispersion.

---

tested. The I–V curves of each of these devices for DC and pulsed conditions are also given in Figure 3.5. The device in Figure 3.5(a) is a standard one-sided CAVET. The gate metal extends all the way across the aperture, so the current does not flow underneath the surface on the drain-side of the gate. The only portion of the AlGaN surface that could affect the charge in the channel is the

region between the source and the gate. Because the electric field in this region is small, the surface states there should not fill up with electrons, so we expect to see no dispersion in this device. We can see from the I–V curves in Figure 3.5(a) that this is indeed what occurs.

In the device shown in Figure 3.5(b), the gate only extends part way across the aperture. This brings the surface on the drain-side edge of the gate closer to the path of current flow, depicted by the blue arrows in Figure 3.5, which we now refer to as the channel. Occupied surface states in this region could potentially modulate the channel, although because the channel does not run directly under this region, we would expect the effect to be relatively small. Indeed, we see in the I–V curves in Figure 3.5(b) that a small amount of dispersion is present in this device.

The device illustrated in Figure 3.5(c) is similar to a HEMT. In this device, the gate is completely offset from the aperture. Current passes directly underneath the AlGaN surface on the drain-side of the gate, so any changes in the potential at this surface will directly affect the amount of charge in the channel. We can see in the I–V characteristics shown in Figure 3.5(c) that this indeed results in a device with very high dispersion.

3.7 Summary

AlGaN/GaN CAVETs were successfully fabricated both with Fe-doped and Mg-doped insulating regions. Although current levels in initial devices were relatively low, improved processing led to devices with maximum currents as high as 750 mA/mm. Additionally, as predicted, optimized GaN CAVETs exhibited negligible DC-RF dispersion. The analysis of dispersion which was performed here showed conclusively that the dispersion prevalent in AlGaN/GaN HEMTs is indeed surface related, and that since there is no surface on the drain side of the gate in the CAVET geometry, DC-RF dispersion is mitigated.

The most prominent issue that was not resolved up to this point was the large amount of leakage that is evident in all of the I–V curves. For high power operation, and especially for high voltage applications, it is critical that leakage currents be extremely small. A complete analysis of leakage currents is conducted in Chapter 4.

References

[1] S. Heikman, S. Keller, T. Mates, S. P. DenBaars, and U. K. Mishra. Growth and characteristics of Fe-doped GaN. *J. Cryst. Growth*, 248:513–7, 2003.

[2] H. Xing, D. S. Green, H. Yu, T. Mates, P. Kozodoy, S. Keller, S. P. Denbaars,

and U. K. Mishra. Memory effect and redistribution of Mg into sequentially regrown GaN layer by metalorganic chemical vapor deposition. *Jpn. J. Appl. Phys., Part 1*, 42(1):50–3, 2003.

[3] J. Baur, K. Maier, M. Kunzer, U. Kaufmann, J. Schneider, H. Amano, I. Akasaki, T. Detchprohm, and K. Hiramatsu. Infrared luminescence of residual iron deep level acceptors in gallium nitride (GaN) epitaxial layers. *Appl. Phys. Lett.*, 64(7):857–9, 1994.

[4] R. Heitz, P. Maxim, L. Eckey, P. Thurian, A. Hoffmann, I. Broser, K. Pressel, and B. K. Meyer. Excited states of Fe^{3+} in GaN. *Phys. Rev. B*, 55(7):4382–4387, 1997.

[5] H. Nakayama, P. Hacke, M. R. H. Khan, T. Detchprohm, K. Hiramatsu, and N. Sawaki. Electrical Transport Properties of p-GaN. *Jpn. J. Appl. Phys., Part 2*, 35:L282–4, 1996.

[6] L. J. van der Pauw. A Method of Measuring the Resistivity and Hall Coefficient on Lamellae of Arbitrary Shape. *Phillips Tech. Rev.*, 20(8):220–4, 1958/59.

[7] Robert Coffie. *Characterizing and Suppressing DC-to-RF Dispersion in AlGaN/GaN High Electron Mobility Transistors*. PhD thesis, University of California, Santa Barbara, 2003.

4

Analysis of parasitic leakage currents

4.1 Introduction

UNFORTUNATELY , all AlGaN/GaN CAVETs with regrown aperture and source regions which have been fabricated to date have exhibited relatively large parasitic leakage currents, often comprising as much as 15% of the total current. These leakage currents resulted in devices that do not pinch off, and they have prevented a meaningful measure of device 3-terminal breakdown voltages, making it impossible to determine whether the large predicted breakdown voltages for a CAVET can be realized. The entire current observed at pinch-off (V_g = – 6 V) in Figure 3.4(b) consists of leakage currents. In a CAVET, the total leakage current is comprised of three elements: (1) electrons from the source passing directly through the insulating layer, (2) electrons from

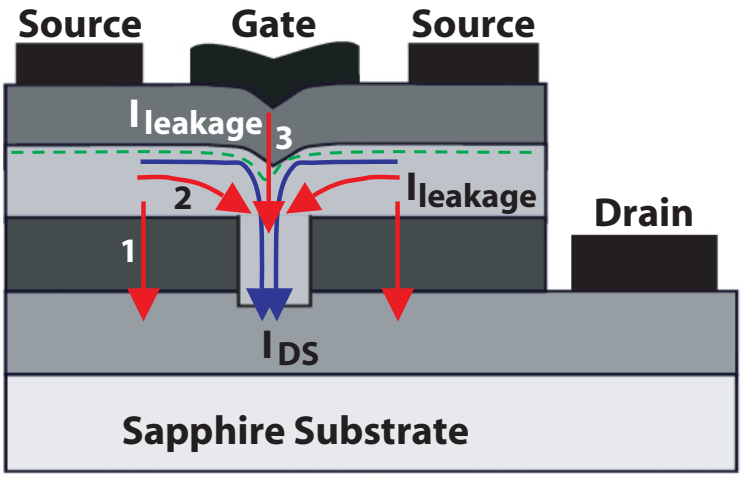

Figure 4.1: Schematic diagram of leakage paths in a CAVET (red arrows represent leakage paths).

---

the source traveling through the aperture but underneath the 2DEG so that they are not modulated by the gate, and (3) electrons traveling from the gate to the drain. A schematic diagram of these leakage paths is illustrated in Figure 4.1.

In order to study leakage currents in CAVETs, it is important to determine how much each of the three components illustrated in Figure 4.1 contribute to the total leakage current. Gate leakage can be measured independently by simply performing a 2-terminal gate-drain I–V measurement. Source leakage through the insulating layer can be approximately measured by performing a

2-terminal source-drain I–V measurement on a device that contains no aperture. Any remaining leakage that is not accounted for by these two components must therefore result from electrons traveling through the aperture but underneath the 2DEG.

By performing the above measurements, all three leakage paths were shown to exist for the device with I–V characteristics illustrated in Figure 3.4. Subsequent studies were performed to determine what was causing each of the leakage paths to exist and how they could be eliminated.

4.2 Source leakage through the insulating layer

Interrupted growth studies confirmed that source leakage through the insulating layer resulted from pits formed on the surface at the onset of regrowth, as the sample was heated to growth temperature. A minimum regrowth temperature of 1160 °C was required in order for the region above the aperture to planarize. However, if the sample was heated to this temperature in 6 liters per minute (slpm) of NH_3 and 6 slpm of H_2 or N_2 at atmospheric pressure without injecting any trimethylgallium (TMGa), as is our standard procedure, then pits formed at

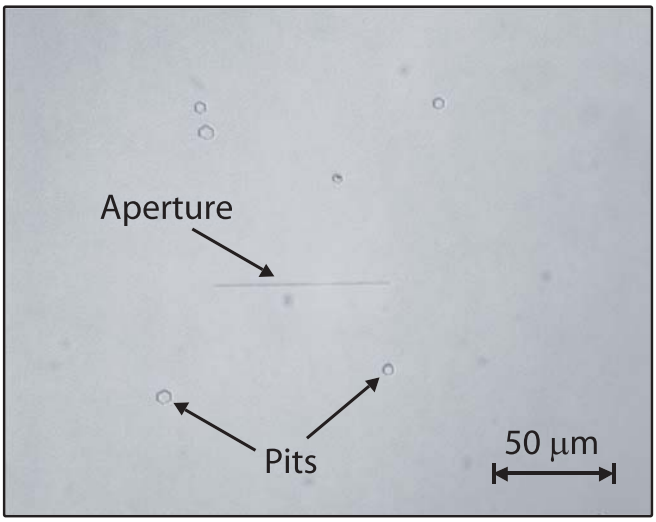

Figure 4.2: Optical photograph of surface after it is heated to regrowth temperature and then immediately cooled back down. Pits and surface roughening can be observed. The straight line indicated in the middle is a 75μm-long aperture.

---

the surface, as seen in Figure 4.2. All devices for which the regrowth was performed under conditions leading to pits exhibited large leakage currents through the insulating layer. Eliminating this leakage path required reducing the reactor pressure, reducing the amount of hydrogen present in the reactor by growing in N_2 and reducing the NH_3 flow, and introducing a small flow of TMGa into the reactor prior to reaching growth temperature. Reducing the temperature also kept the pits from forming; however, for temperatures less than 1160 °C, the

material above the aperture did not always planarize, in which case gate leakage was much more severe. In order to ensure that pits did not form during regrowth, subsequent devices were heated to regrowth temperature in 3 slpm of NH_3 and 9 slpm of N_2 at a pressure of 300 torr. Additionally, a small amount of TMGa was injected into the reactor while the temperature was ramped from 1050 to 1160 °C. Figure 4.3 shows the I–V characteristics of a device grown under conditions that were optimized to eliminate pits in the insulating layer. All devices for which the regrowth was performed under these optimized conditions exhibited negligible leakage through the insulating layer.

4.3 Source leakage underneath the 2DEG

It was stated earlier that the conductivity of the 2DEG needs to be much higher than that of the adjacent bulk GaN directly below the 2DEG to ensure current flow through the 2DEG rather than through the bulk GaN. Source leakage underneath the 2DEG occurred when these conditions were not met. In addition, source leakage underneath the 2DEG can can also occur at large values of V_{DS} if the gate-overlap length L_{go} is too small (see Figure 2.4). Leakage through

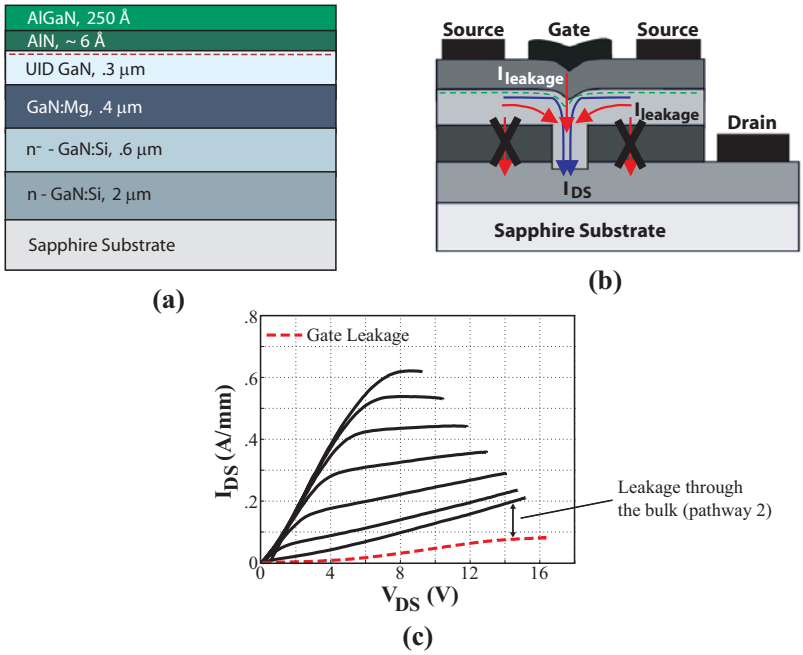

Figure 4.3: Device in which regrowth conditions were optimized to eliminate surface pitting while simultaneously allowing the surface above the aperture to become nearly planar. (a) Device layer structure, (b) active leakage paths, and (c) device I–V characteristics. The dashed curve in (c) was taken without contacting the sources; thus it is a measure of the total gate leakage in this device.

---

this path was reduced by keeping the UID layer as thin as possible, insuring that it was fully depleted all the way up to the 2DEG. The device illustrated in Figure 4.3 had a relatively thick UID GaN layer. The resulting source leakage current in this device is simply the difference between the curve in which the device is pinched off [bottom black curve in Figure 4.3(c)] and the gate leak-

age [dashed curve in Figure 4.3(c)]. For UID layers with thickness $\leq$ 1700 Å, no leakage through this path was observed for drain voltages of up to $\sim$ 50 V, which was the breakdown voltage of those devices. It is possible that in devices with larger breakdown voltages, leakage through this path may be observed at higher drain voltages. The compromise is that if the UID layer is too thin, the mobility of the 2DEG channel is reduced, and the region above the aperture does not always planarize as well, resulting in more severe gate leakage.

4.4 Gate Leakage

As stated earlier, material inside as well as above the aperture region was not grown on the c-plane, but rather on an inclined or vertical facet. Other studies have found evidence that GaN which is grown on facets other than the $<$0001$>$ plane tends to incorporate larger concentrations of n-type impurities [1, 2]. We therefore believe that the material directly beneath the gate is highly n-type, resulting in a leaky gate Schottky barrier [see Figure 4.4(a)]. Because the peak electric field in a CAVET is located directly beneath the gate, this n-type doping also causes an increase in the peak field, which limits the breakdown voltage in

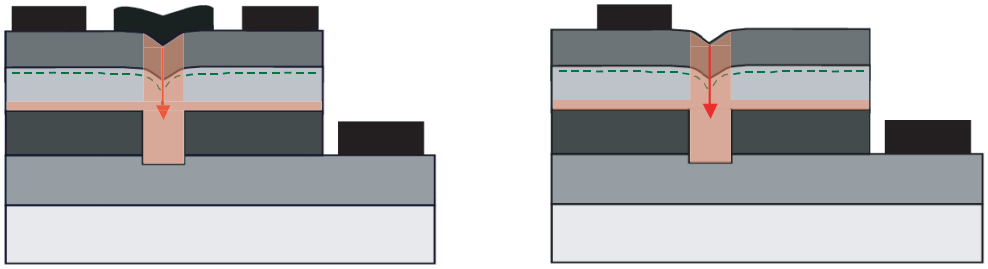

Figure 4.4: (a) Schematic of CAVET. Shaded region is unintentionally doped highly n-type during regrowth. (b) Test structure with a gate that is offset from the aperture.

---

these devices. It is therefore important to reduce the n-type doping level inside and above the aperture region not only to eliminate gate leakage but also to achieve high breakdown voltages.

Although it is possible that gate leakage could result from the enhanced electric fields that are caused by the indentation in the surface underneath the gate, our hypothesis that it is the enhanced doping in the regrown regions close to the aperture (shaded regions in Figure 4.4) is supported by the fact that in test structures where the gate is offset from the aperture, gate leakage is eliminated while breakdown voltage remains the same [see test structure in Figure 4.4(b)]. If gate leakage had resulted from the enhanced fields caused by the indentation

in surface, an increase in the breakdown voltage would be expected when the gate was offset from the aperture.

In order to eliminate gate leakage, we attempted to find growth conditions that would cause the surface to completely planarize almost immediately during regrowth. Conditions that favored planarization included reducing the V/III ratio and increasing the temperature. However, the higher regrowth temperatures required to planarize the surface also resulted in increased source leakage due to the formation of pits while the sample was being heated. At temperatures in which source leakage was eliminated, the surface never fully planarized, so gate leakage was still present in all devices.

4.5 Summary

Leakage currents were found to be a major issue in AlGaN/GaN CAVETs, preventing realization of the high breakdown voltages predicted for CAVETs. The various leakage paths present in CAVETs were addressed in this chapter, and conditions were identified which eliminated both of the paths associated with source leakage. However, because of the uncontrollably high n-type doping of

the material inside and above the aperture, gate leakage could not be eliminated.

In order to eliminate gate leakage as well as to achieve the high predicted breakdown voltages in a CAVET, it is necessary to be able to better control the doping both within the aperture and underneath the gate. This was later achieved by using an ion implantation to define the insulating layer, as discussed in Chapter 5. In addition, an insulator underneath the gate could be used to further reduce gate leakage and increase breakdown voltage. This technique has previously been successfully implemented in the fabrication of high breakdown GaN HEMTs [3]. Despite the problems with gate leakage, working devices were still fabricated.

References

[1] S. Heikman, S. Keller, S. P. DenBaars, U. K. Mishra, F. Bertram, and J. Christen. Non-planar Selective Area Growth and Characterization of GaN and AlGaN. *Jpn. J. Appl. Phys., Part 1*, 42(10):6276–83, 2003.

[2] S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra. Oxygen doping of c-plane GaN by metalorganic chemical vapor deposition. *Phys. Status Solidi C*, 0(7):2557–61, 2003.

[3] N. Zhang, B. Morgan, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma. Kilovolt AlGaN/GaN HEMTs as switching devices. *Phys. Status Solidi A*, 188(1):213–17, 2001.

5

AlGaN/GaN CAVETs with ion implanted insulating regions

5.1 Introduction

ALTHOUGH promising results were achieved for CAVETs with regrown apertures, ultimately problems with gate leakage and low breakdown voltages proved to be insurmountable. In order to fabricate a leakage free device and increase breakdown, it is necessary to utilize a process in which doping levels in the aperture region and below the gate can be precisely controlled. One way to achieve this goal is by using ion implantation to define the insulating layer.

The primary advantage offered by a process which utilizes an ion implantation is that the entire growth is planar, so doping levels in all active device layers can

be accurately controlled. For the fabrication of CAVETs with ion implanted insulating layers, two approaches are possible. The first option is to grow the entire device layer structure, then implant through the 2DEG, and finally try to heal the damage done to the source region with a thermal anneal. This process is illustrated schematically in Figure 5.1. The second option is to first grow the drain and aperture regions, then perform the implantation, and finally regrow the source region. This process is shown in Figure 5.7 and described in greater detail in §5.3. The first approach is very appealing because it allows for a much simpler process as well as the possibility of a gate which is self-aligned to the aperture. However, initial attempts at this process appeared to indicate that recovery of the 2DEG after the implant would be extremely difficult if not impossible. The second approach, for which the process only required minor modifications from ones previously used in this work, was therefore used.

5.2 Ion implantation

Ion implantation has been used extensively in III-V semiconductors such as GaAs and InP to achieve current confinement through the selective disordering

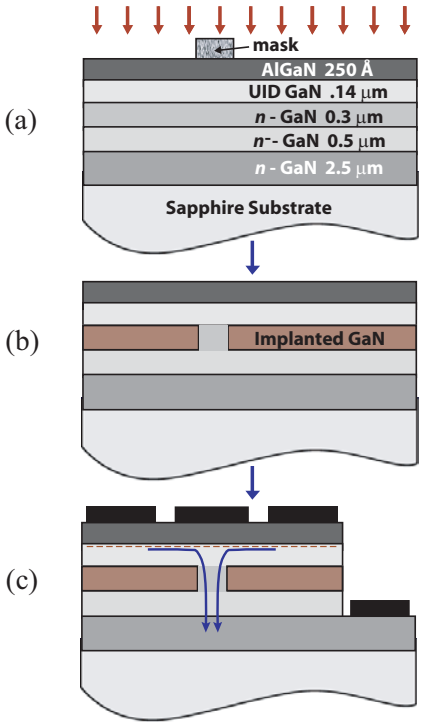

Figure 5.1: Process flow for ion implanted CAVETs with no regrowth. (a) Structure is grown, implant mask is deposited, and implant is performed. (b) Implant mask removed, sample annealed to recover 2DEG. (c) Devices are processed.

---

of material [1]. Although implantation of GaN has been reported, research has mostly focused on doping with magnesium [2] or silicon [3] ions. Implantation of GaN for the purpose of disordering has been reported for nominally undoped material using iron [4], for n-type material using hydrogen, helium, and nitrogen species [5], and for p-type material using aluminum [6].

5.2.1 Preliminary optimization

In designing an ion implantation process, it is necessary to first decide on an implant species and then optimize the implant conditions to achieve the necessary profile. The choice of implant species depends on subsequent processing. Although lighter ions such as hydrogen and helium can cause disordering, their implant profiles may change during any subsequent anneals, such as in a regrowth. Heavier species, such as aluminum, have been shown to result in a very thermally stable implant [6]; aluminum was therefore chosen for this work.

The depth and profile of the ion implant for a given set of implant conditions can be modelled by using SRIM2003 (Stopping Range of Ions in Matter). This simulation program takes into account the density of the material being implanted as well as the mass and energy of the implanted species. However, it does not account for the crystal structure of the semiconductor. Although in most semiconductors this is not an issue, significant channeling of the implanted species can occur in wurtzite GaN as a result of the c-plane orientation of the material, resulting in a much deeper and more smeared-out implant profile than would otherwise be predicted [6, 7]. In an effort to suppress this channeling,

angled implantations were performed in this study.

The conductivity of the implanted region is ultimately determined by the amount of damage to that layer, which depends on both the energy of the implanted ions and the ion dosage. In previous studies, the conductivity of layers implanted with aluminum was measured for doses of 10^{12} to 10^{15} cm^{-2} and an energy of 180 keV [6]. In these studies, it was determined that doses of at least $\sim 10^{14}$ cm^{-2} were required for the implanted layers to be adequately insulating. The implant energy selected for this work was 90 keV, the dose was 10^{15} cm^{-2}, and the implant angle was 7°. From SRIM simulations, for these conditions the expected average ion range was 820 Å with a straggle of 370 Å, and the expected lateral range was 320 Å with a straggle of 400 Å.

The simulated depth profile obtained for these conditions using SRIM along with the experimentally measured results are illustrated in Figure 5.2. Experimental results were obtained by performing secondary ion mass spectroscopy (SIMS) measurements on device structures. The measured profile was extremely close to the theoretical predictions, indicating that channeling of the implanted species was effectively suppressed by the 7° implantation angle.

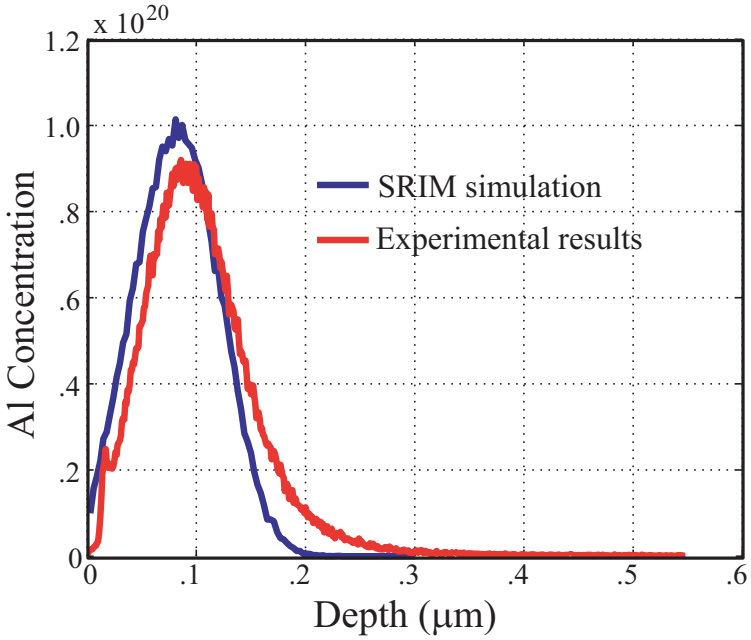

Figure 5.2: SRIM simulation (blue) along with SIMS profile (red) of an angled Al implantation into GaN. The implant energy was 90 keV, the dose was 10^{15} cm^{-2}, and the implant angle was 7°.

5.2.2 Regrowth

After the ion implantation, an MOCVD regrowth was performed to deposit the source region. Regrowth conditions were identical to those used for devices with Mg-doped insulating layers to ensure that source leakage was suppressed. The regrowth also served the purpose of providing high temperature anneal con-

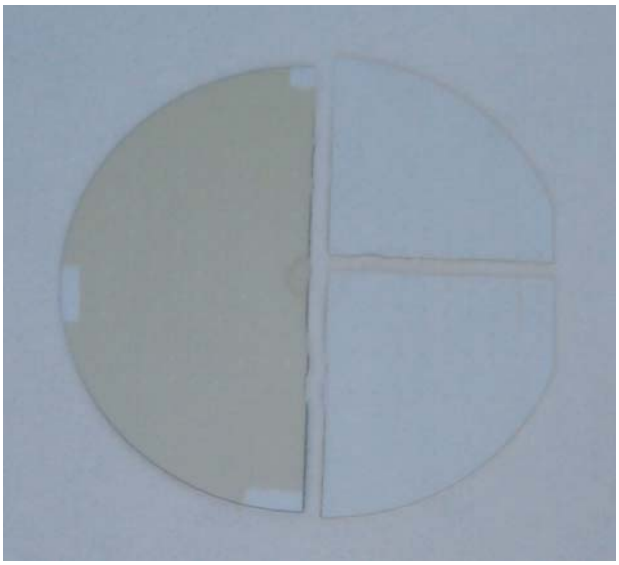

Figure 5.3: Optical photograph of implanted material before (left) and after (right) regrowth. As-implanted material was yellowish in appearance. After regrowth, the wafer was clear again.

---

ditions during which some of the implant damage was healed. As shown in Figure 5.3, prior to regrowth, implanted areas on the wafer were yellowish in color due to a high density of defect levels that resulted from implant damage [6]. However, after regrowth, the wafer became clear again, implying that some of the damage incurred by the crystal during implantation was healed.

5.2.3 Ohmic contacts above the ion implanted layer

For CAVET structures with implanted insulating regions, contacting the 2DEG without also contacting the n-type drain region was not completely straightforward. The standard process at UCSB for contacting the 2DEG in an AlGaN/GaN heterostructure, which was used previously in this work, is to deposit a Ti/Al/Ni/Au contact on top of the AlGaN and then anneal the structure, so that the metal and the underlying material mix and form an alloy. When this same ohmic process was attempted in the ion implanted CAVET structure, the source metal was found to also contact the n-type drain region, effectively shorting the source to the drain. This occurred for implant doses of 10^{14} cm^{-2} and 10^{14} cm^{-2}. We hypothesize that because of the high implant doses, Al clusters may have formed in the implanted layer. Then during the ohmic anneal, the aluminum in the implanted layer reacts with the ohmic metal, resulting in a conductive alloy that extends from the source contact all the way down to the drain region.

In order to prevent the source ohmics from contacting the drain region, it was necessary to use a non-alloyed ohmic contact. To accomplish this, it was neces-

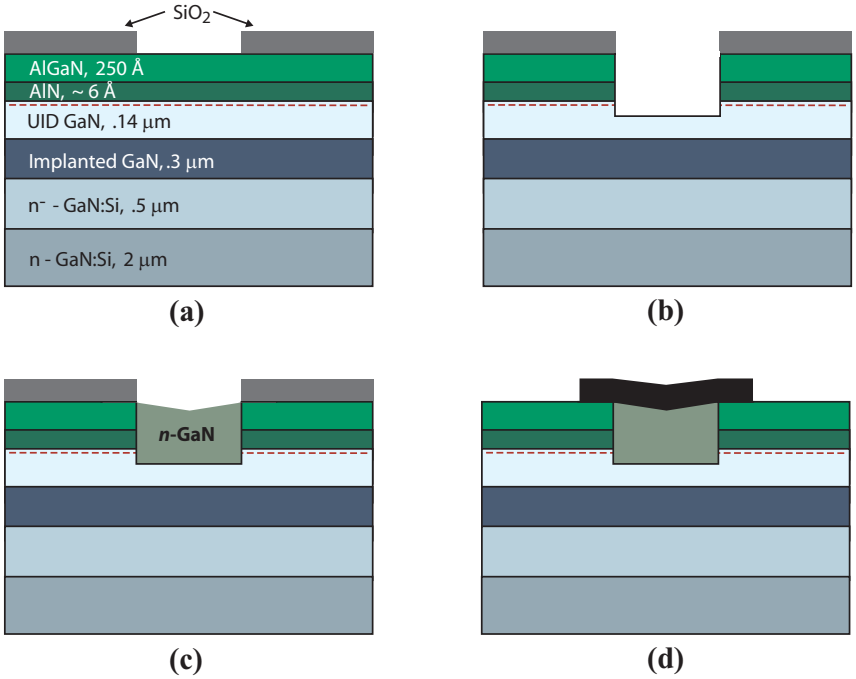

Figure 5.4: Process flow for non-alloyed ohmic contacts. (a) SiO_2 mask is deposited. (b) RIE etch. (c) Regrowth of source region. (d) SiO_2 removed, ohmic metal deposited.

---

sary to regrow n-type material below the metal so that an ohmic contact could be formed without annealing. The entire process for the contact, which was modelled after the technique developed by Heikman *et al.* for regrown contacts in AlGaN/GaN HEMTs [8], is outlined in Figure 5.4.

First, an SiO_2 etch mask was deposited to expose the source contact area, as

shown in Figure 5.4(a). Large areas near the edge of the device mesas were also left uncovered. Next, Cl_2 RIE was used to etch a trench through the AlGaN and into the underlying GaN, as illustrated in Figure 5.4(b). The trenches were 2 μm wide and $\sim$ 0.1 μm deep. The wafers were then placed back in the MOCVD reactor and annealed in NH_3 and TMGa for 2 minutes at 1160 °C. The trenches filled with GaN extremely quickly as a result of mass transport of material from the large uncovered areas near the device mesas into the narrow trenches. A diagram of the resulting profile is shown in Figure 5.4(c). The material inside the trenches was highly n-type, as silicon and possibly oxygen autopdoping resulted from the SiO_2 mask material. Finally, the SiO_2 mask was removed, and Al/Au (300/3000 Å) was deposited on top of the regrown material to form an ohmic contact, as illustrated in Figure 5.4(d). Contact resistance, which was characterized by TLM, was measured to be 1.0 Ω-mm. The contacts were slightly rectifying, as can be seen in device I–V curves illustrated in Figure 5.9(b), although they were still adequate for both DC and RF device characterization. However, for future work, improvements in non-alloyed ohmic contacts would be highly desirable.

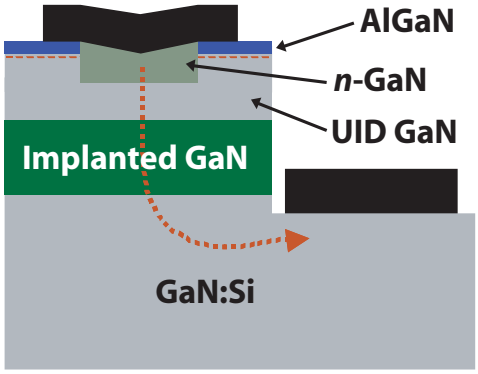

Figure 5.5: Diode structure fabricated to evaluate insulating properties of a GaN layer implanted with aluminum ions.

5.2.4 Characterization of the ion implanted layer

In order to evaluate the resistivity of the implanted layer, the diode structure illustrated in Figure 5.5 was fabricated. The 2DEG was contacted with a regrown non-alloyed contact, as described in §5.2.3, to ensure that it remained isolated from the underlying n-type drain region below the implanted layer. Diode I–V measurements were performed to quantify leakage through the insulating layer. Less than 5 mA/mm^2 of current was measured for all biases below breakdown, indicating that the implanted layer was sufficiently insulating within the operating range of devices. A comparison of leakage currents for Fe-doped, Mg-doped, and ion implanted insulating layers is shown in Figure 5.6.

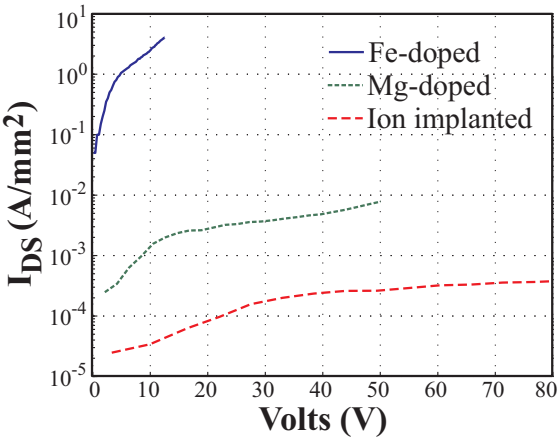

Figure 5.6: Comparison of leakage currents through insulating layer for devices with Fe-doped, Mg-doped, and ion implanted insulating layers.

5.3 Device process for ion implanted CAVETs

The following section describes the entire fabrication process for a CAVET with an ion implanted insulating region. Because many steps in the processing are identical to those of devices with Mg- and Fe-doped insulating layers or were described previously in this chapter, detailed descriptions are only given for new procedures.

Fabrication began with the growth of the initial base structure, which consisted of a 2.5 μm n-type GaN drain layer ($N_d \sim 1\times10^{18}$), a 0.5 μm n^- GaN drift re-

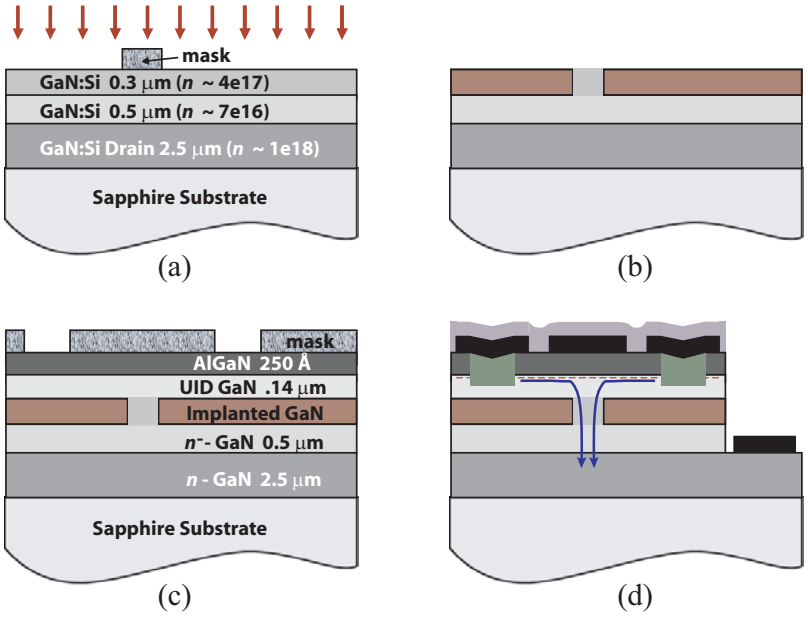

Figure 5.7: Process flow for AlGaN/GaN CAVETs with ion implanted insulating layers. (a) Initial growth, implant mask is deposited, and implant is performed. (b) Implant mask is removed. (c) Regrowth is performed and mask for ohmic contact regrowth is deposited. The Al composition in the AlGaN $x_{Al} = 30\%$. Although not pictured, a 6 Å AlN layer was included beneath the AlGaN. (d) Ohmic regrowth is performed, mask is removed, and devices are processed.

---

gion ($N_d \sim 7{\times}10^{16}$), and a 0.3 μm n-type GaN layer for the aperture region ($N_d \sim 4{\times}10^{17}$). The structure is illustrated in Figure 5.7(a). Next, a Ti/Au/Ni (400/2400/200 Å) implant mask was deposited, and an aluminum ion implantation was performed to define the insulating layer. The implant conditions were given in §5.2.1, and the resulting profile is shown schematically in Figure 5.7(b).

The wafer was then covered in photoresist, the area containing the alignment marks was exposed, and the Ti/Au/Ni which defined the alignment marks was used as an etch mask so that aligment marks would still be visible after the implant mask was removed. A 2000 Å RIE etch was performed to define the alignment marks, and the implant mask was then removed using a Au etchant and buffered HF. Alignment marks were then covered by sputtering AlN, after which the wafer was placed back into the MOCVD chamber and a maskless regrowth was performed. 1400 Å of UID GaN was grown, followed by a 6 Å AlN layer and a 250 Å AlGaN cap, resulting in the structure shown in Figure 5.7(c). Next, a SiO_2 mask was evaporated, and trenches in the source region were etched and regrown, as described in §5.2.3. The SiO_2 mask was then removed in buffered HF, and a device mesa for the source and gate region was formed with Cl_2 RIE. Al/Au (300/3000 Å) were then evaporated to form ohmic source and drain contacts. Because the contacts were not alloyed, they were slightly rectifying, as can be seen in the I–V curves in Figure 5.9. Next, the area on the device mesa where the source and gate probe pads sit was isolated from the source region. A 600 Å Cl_2 RIE etch was performed to remove the AlGaN and some of the underlying GaN, followed by a 2500 Å electron beam SiO_2 depostion. After this,

300/3500 Å of Ni/Au was evaporated for a gate metallization. Next, Ti/Au (300/3000 Å) was evaporated for source and gate probe pads. Finally, an 800 Å SiN passivation layer was deposited by plasma enhanced chemical vapor deposition (PECVD). The final device structure is illustrated in Figure 5.7(d). Devices were tested completely prior to the SiN deposition, and then retested after passivation.

5.4 Design parameters for aperture region

For CAVETs with implanted insulating layers, epitaxy of the material inside the aperture region occurs during the initial growth, rather than during regrowth. Because the properties of the material in the aperture region are highly controllable with this process, the doping level of this material can be adjusted to optimize device performance. The doping must be high enough so that the conductivity of this region is much larger than that of the 2DEG, but levels which are too high result in low breakdown voltages. The conductance of the aperture region is also proportional to the aperture length L_{ap}, so devices with smaller apertures may require higher doping levels in the aperture region. It should be

noted that the actual device aperture length is ~ 0.1 μm smaller than the length of the implantation mask due to the expected lateral range and straggle of the implanted ions. The doping level chosen for these experiments was $\sim 4\times10^{17}$, and aperture lengths ranged from 0.6 μm to 2 μm.

5.5 Device characterization

5.5.1 SIMS analysis

In order to ensure proper device performance, it is important that the n-type layer grown for the aperture region be at least as thick as the maximum penetration depth of the implanted ions. If the implanted ions penetrate all the way into the n^- layer, then the conductivity of the bottom section of the aperture region could potentially be too low, resulting in non-ideal DC performance. Secondary ion mass spectroscopy (SIMS) was carried out on the device structures to verify that the implantation conditions were indeed compatible with the layer design. The results are illustrated in Figure 5.8. Additionally, as expected, a large spike in the Si concentration could be observed at the regrowth interface.

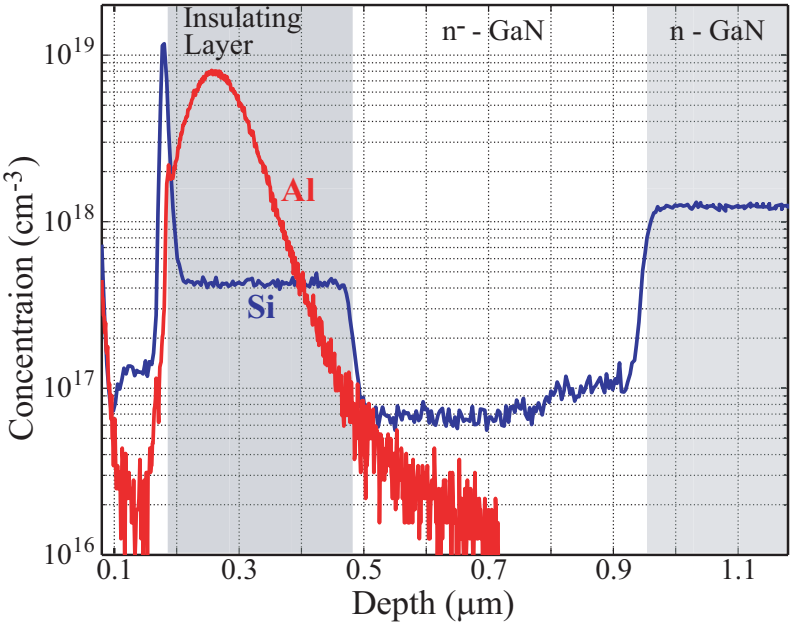

Figure 5.8: SIMS analysis of device layer structure, verifying that the implantation conditions were compatible with the layer design. A large spike in the Si concentration occurred at the regrowth interface.

5.5.2 Device results

The device layer structure, as well as DC and pulsed I_{ds}–V_{ds} characteristics of an unpassivated CAVET with an ion implanted insulating layer are illustrated in Figure 5.9. This device had a maximum source-drain current I_{max} of 780 mA/mm, a pinch-off voltage V_p of – 5 V, and an extrinsic transconductance g_m of $\sim$ 135 mS/mm at $I_{ds} \sim$ 600 mA/mm and $V_{ds} \sim$ 7 V. Although the total current

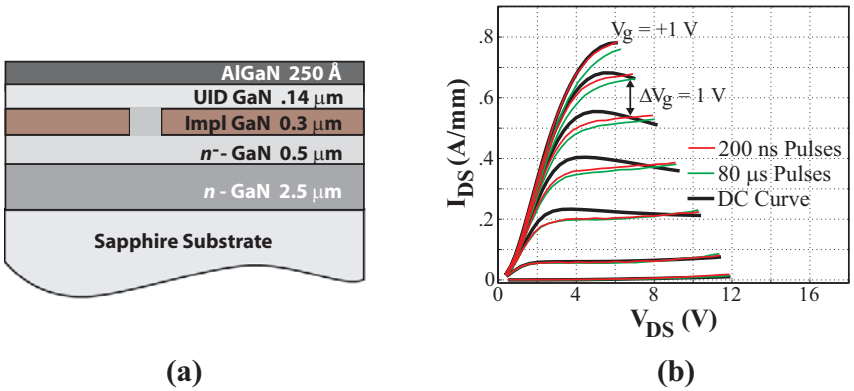

Figure 5.9: (a) Device layout and (b) I–V characteristics of an unpassivated CAVET with an implanted insulating layer. For this device, $L_{ap} = 1.4$ μm and $L_{go} = 1.2$ μm.

---

in these devices was only slighly higher than in previous ones, leakage currents were much lower, so current flow through the 2DEG was significantly higher. However, even though leakage was reduced in these devices, it was not completely eliminated. An analysis of the leakage currents revealed that all leakage in these devices originated at the gate; source leakage was entirely suppressed. Gate leakage still prevented measurements of the 3-terminal breakdown voltage, but 2-terminal breakdown was measured to be $\sim$ 60 V. A comparison of the DC device characteristics to those where the gate was pulsed from pinchoff to their final value revealed that these devices exhibit very little dispersion for

80 μs as well as 200 ns pulse widths. The small amount of dispersion was shown to be related to traps in the implanted layer rather than the AlGaN surface. A more detailed analysis of dispersion in these devices is presented in §5.6. Device DC electronic characteristics were found to be independent of L_{ap} for aperture lengths ranging from 0.8 μm to 2 μm. In devices where L_{ap} was less than 0.8 μm, current levels were slightly lower, implying that the conductance of the aperture region was comparable to that of the 2DEG.

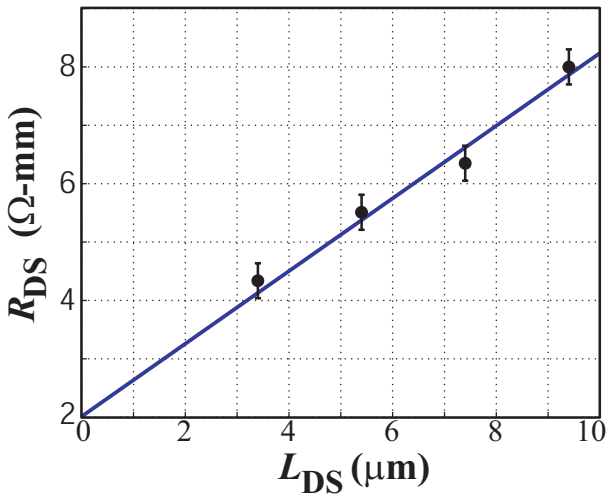

Figure 5.10: TLM measurements of 2DEG. The contact resistance (R_s = (y–int)/2) was 1.0 Ω-mm, and the $q{\cdot}\mu_n{\cdot}n_s$ product, which is proportional to the inverse of the slope, was $1.6{\times}10^{-3}$ $(\Omega/\square)^{-1}$.

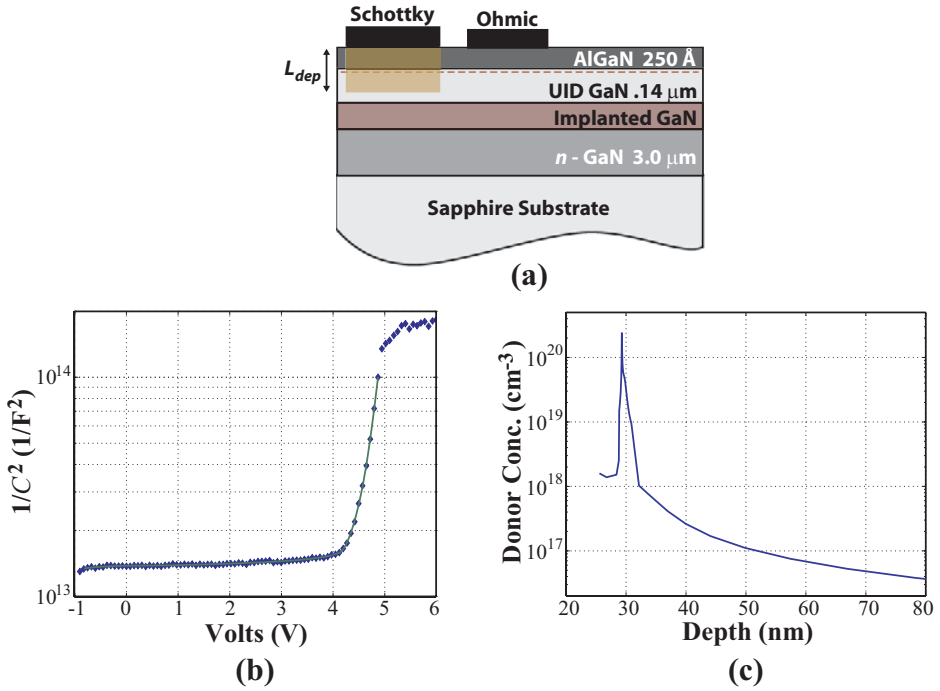

Figure 5.11: (a) Diode structure for C–V measurement, (b) C–V characterization, and (c) charge distribution. The sheet charge n_s in the 2DEG, which was determined by integrating under curve (c), was calculated to be 9.8×10^{12} cm^{-2}.

5.5.3 Characterization of the 2DEG

Because of the difficulties in contacting the 2DEG without also contacting the drain region, Hall measurements were not performed on these devices. Instead, the $\mu_n \cdot n_s$ product was determined from TLM measurements, and afterwards the

sheet charge was extracted from C–V analysis. The results from the TLM measurements are illustrated in Figure 5.10, and those from the C–V measurements are shown in Figure 5.11. A sheet charge of 9.8×10^{12} cm^{-2} and a mobility of 1027 cm^2/V·s was extracted for the 2DEG. Compared to HEMTs with similar AlGaN layers, the charge and mobility of the 2DEG in the CAVET were both relatively low, probably due to the close proximity of the 2DEG to the implanted layer and the regrowth interface.

5.6 Analysis of DC-RF dispersion

When devices are under bias, self heating causes a reduction in the measured output currents. Although self heating effects are minimal in devices grown on SiC, which has a large thermal conductivitiy, the effects are quite evident in devices grown on sapphire, which is a poor thermal conductor. Self heating effects are reduced when the pulse width used in the I–V measurements is reduced. Therefore, when device characteristics are dominated by self heating, shorter pulse widths result in larger output currents, while in devices dominated by dispersion, shorter pulse widths result in smaller currents. In other words, if

a device exhibits no dispersion, shorter pulse widths lead to less self heating and result in slightly larger output currents. If a device exhibits large dispersion, then shorter pulse widths result in smaller output currents.

The device in Figure 5.9 represents the unusual case in which a very small amount of dispersion is present, so neither dispersion nor self heating dominates. As a result, the current for 80 μs pulsed curves is slightly less than that of the DC curves due to the small amount of dispersion in this device. However, when the pulse width is reduced from 80 μs to 200 ns, the current actually increases, since self heating effects are reduced.

In § 3.6, it was shown that in a CAVET, dispersion related to the AlGaN surface is mitigated. The dispersion observed in this device was therefore attributed to traps in the insulating layer that were induced by implantation damage. A series of devices similar to those in Figure 3.5 were again fabricated to verify this assumption. These devices are illustrated in Figure 5.12. Throughout the remainder of this dissertation, these devices will be referred to as Device A, Device B, and Device C. Additionally, after being tested, the devices were passivated and then retested to further confirm the results.

The I–V characteristics of the three devices in Figure 5.12 are illustrated in

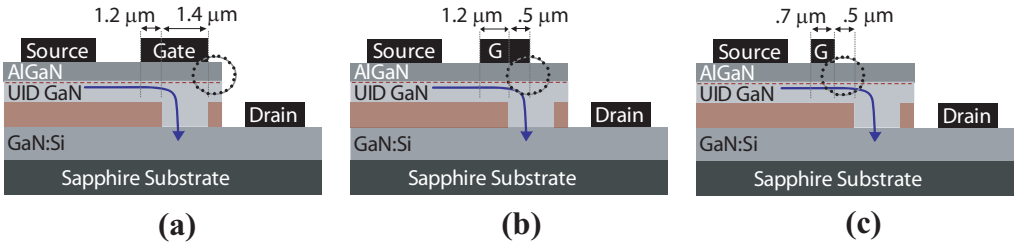

Figure 5.12: Three CAVET structures fabricated in order to investigate DC-RF dispersion in ion implanted CAVETs. (a) Device A. Gate completely covers the aperture. (b) Device B. Gate partially covers the aperture, drain-side edge of gate is near the current path. (c) Device C. Gate is completely offset from the aperture.

Figure 5.13. The upper curves were taken before passivation was performed, and the lower curves were taken after passivation. For unpassivated devices, results were similar to previous devices. As the AlGaN surface on the drain side of the gate was brought closer to the channel, surface-related dispersion increased. However, in Device A, for which the surface should not affect the I–V characteristics, there was still a small amount of dispersion. This dispersion was attributed to traps in the ion implanted layer, and could perhaps be reduced by decreasing the ion dose.

To verify that the dispersion in Device A was not related to the surface, the three devices were passivated and then retested. Passivation should eliminate all

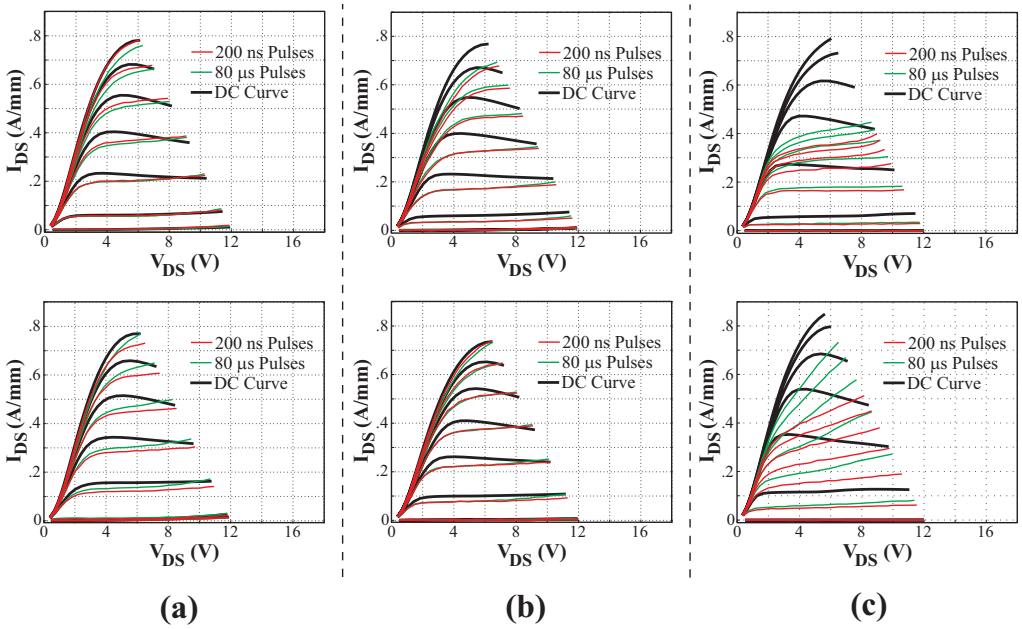

Figure 5.13: I–V characteristics of the devices in Figure 5.12. (a) Device A, (b) Device B, and (c) Device C. The top curves were taken prior to passivation, and the bottom curves were taken after passivation.

surface related dispersion, so any dispersion measured after passivation should not be surface related. We can see that in Device A, I–V characteristics were unaffected by passivation, and in Device B, passivation led to I–V characteristics identical to those of Device A, indicating that the dispersion observed in Device A was not cause by AlGaN surface states. In Device C, for which surface related dispersion was severe, an improvement in the I–V characteristics after

passivation was observed, but some dispersion was clearly still present. Because passivation is a very sensitive process, it is possible that although surface related was reduced after passivation, it was not completely eliminated. However, another possible explanation for the dispersion observed after passivation in Device C is that the implanted region may have been subject to very high fields in this device, since the current saturation region lies above the implanted region rather than above the aperture. If this is the case, the observed dispersion results from traps in the implanted region, and not from the surface.

5.7 Breakdown and leakage

The original motivation for fabricating CAVETs with implanted layers was to be able to control the doping levels of the material directly below the gate so that gate leakage could be eliminated and large breakdown voltages achieved. Leakage and breakdown were measured and analyzed for the three devices in Figure 5.12, both before and after passivation. The results are given in Table 5.1.

Despite extremely low leakage currents measured in Device C, Devices A and B still had a considerable amount of leakage, although even in these devices

	Device A	*Device B*	*Device C*
Leakage at $V_D = 14$ V	20 mA/mm	15 mA/mm	$<$ .04 mA/mm
2-terminal V_{br} before passivation	60 V	60 V	110 V
2-terminal V_{br} after passivation	60 V	60 V	80 V
3-terminal V_{br} before passivation	N/A	N/A	85 V
3-terminal V_{br} after passivation	N/A	N/A	35 V

Table 5.1: Leakage and breakdown characteristics of devices with implanted layers

leakage was much lower than in previous ones. The leakage analysis described in Chapter 4 was performed on these devices to determine which leakage paths were prominent. For all three devices, no detectable amount of source leakage could be measured. In Devices A and B, the total observed leakage current was determined to be gate leakage, and leakage was slightly larger in Device A than in Device B (these trends were consistent across the entire wafer). This suggests that the material above the aperture had still somehow been doped unintentionally, so that devices in which the gate metal lay directly above the aperture still exhibited significant gate leakage. It is possible that unintentional doping in this region could have resulted from contamination from the implant mask if the mask had not been completely removed prior to regrowth, although further investigation is necessary to fully characterize and resolve this problem.

In GaN HEMTs, the breakdown voltage typically decreases after passivation. This occurs because in unpassivated HEMTs, surface states near the drain side edge of the gate charge up as the device is biased, causing the high electric field region to spread over a larger distance and thus reducing the peak electric field. After passivation, surface states can no longer charge up, so the peak electric field increases, resulting in a reduction of V_{br}. In a standard CAVET, such as Device A, we expect the breakdown voltage to remain unchanged after passivation, since surface states should not charge up even before passivation. Unfortunately, in both Device A and Device B, gate leakage was too high to measure 3-terminal breakdown voltages, and 2-terminal breakdown was limited to 60 V, also because of leakage. This value did not change after passivation, indicating that breakdown was not being limited by surface effects. However, these same measurements should be repeated on devices with no leakage to verify that breakdown remains constant even when it is not limited by gate leakage. In Device C, for which gate leakage was very low, breakdown characteristics were similar to those of a GaN HEMT, which was to be expected. Before passivation, the 2-terminal and 3-terminal breakdown voltages were measured to be 110 V and 85 V, respectively, while after passivation they reduced to 80 V and 35 V.

To reduce gate leakage to acceptable levels for standard CAVETs, an insulator underneath the gate metal is probably necessary. A very thin ($\sim$ 60 Å) layer of SiO_2, which had been deposited by electron beam evaporation, had previously been used by Zhang *et al.* to reduce gate leakage in high breakdown GaN HEMTs [9]. However, this same structure did not improve the leakage characteristics of these CAVETs. It is probably necessary to first reduce leakage below a certain threshold before the benefits of the SiO_2 layer can be realized. However, Chini *et al.* [10] have shown that gate leakage in GaN MESFETs, which was previously very large, could be greatly reduced by inserting a 25 Å layer of MOCVD grown SiN underneath the gate metal. This same process could also be used in a CAVET to reduce gate leakage. Since the MOCVD SiN can be deposited during the regrowth, it does not add any significant steps to the overall process.

5.8 Summary

CAVETs with ion implanted insulating layers were successfully fabricated and tested. Maximum drain currents as high as 780 mA/mm were measured, and

leakage was much less severe than in previous devices. However, gate leakage was still not completely mitigated and led to relatively low breakdown voltages. By placing a thin layer of MOCVD grown SiN atop the AlGaN surface underneath the gate metal, it should be possible to eliminate gate leakage and thus achieve larger breakdown voltages.

References

[1] J. P. Reithmaier and A. Forchel. Focused ion-beam implantation induced thermal quantum-well intermixing for monolithic optoelectronic device integration. *IEEE Journal of Selected Topics in Quantum Electronics*, 4(4):595–605, 1998.

[2] A. Wenzel, C. Liu, and B. Rauschenbach. Effect of implantation-parameters on the structural properties of Mg-ion implanted GaN. *Materials Science and Engineering B - Solid State Materials for Advanced Technology*, 59(1-3):191–4, 1999.

[3] X. A. Cao, J. R. LaRoche, F. Ren, S. J. Pearton, J. R. Lothian, R. K. Singh, R. G. Wilson, H. J. Guo, and S. J. Pennycook. Implanted p-n junctions in GaN. *Solid-State Electronics*, 43(7):1235–8, 1999.

[4] C. Liu, E. Alves, A. D. Sequeira, N. Franco, M. F. da Silva, and J. C. Soares. Fe ion implantation in GaN: Damage, annealing, and lattice site location. *Journal of Appl. Phys.*, 90(1):81–6, 2001.

[5] S. C. Binari, H. B. Dietrich, G. Kelner, L. B. Rowland, K. Doverspike, and D. K. Wickenden. H, He, and N implant isolation of n-type GaN. *Journal of Appl. Phys.*, 78(5):3008–11, 1995.

[6] Tal Margalith. *Development of Growth and Fabrication Technology for Gallium Nitride-Based Vertical Cavity Surface Emitting Lasers*. PhD thesis, University of California, Santa Barbara, 2002.

[7] E. D. Haberer, C.-H. Chen, A. Abare, M. Hansen, S. Denbaars, L. Coldren, U. Mishra, and E. L. Hu. Channeling as a mechanism for dry etch damage in GaN. *Appl. Phys. Lett.*, 76(26):3941–3, 2001.

[8] S. Heikman, S. Keller, B. Moran, R. Coffie, S. P. DenBaars, and U. K. Mishra. Mass transport regrowth of GaN for ohmic contacts to AlGaN/GaN. *Phys. Status Solidi A*, 188(1):355–8, 2001.

[9] N. Zhang, B. Morgan, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma. Kilovolt AlGaN/GaN HEMTs as switching devices. *Phys. Status Solidi A*, 188(1):213–17, 2001.

[10] A. Chini, D. Buttari, S. Keller, and U. K. Mishra. to be published.

6

Small Signal RF performance of the AlGaN/GaN CAVET

6.1 Introduction

ONE of the primary objectives behind the research into the AlGaN/GaN CAVETs was to investigate their potential as high power, high frequency transistors. Fundamental material properties of GaN, such as a high saturated electron velocity, a large critical breakdown field, and good thermal stability make GaN transistors an excellent candidate for these applications. Additionally, the ability to form a 2DEG near the interface of an AlGaN/GaN heterojunction allows for very high electron mobilities μ_n while maintaining a large channel charge n_s. AlGaN/GaN HEMTs on SiC have already been demonstrated with output powers as high as 30 W/mm at 8 GHz [1]. This power density is

more than an order of magnitude higher than that of state-of-the-art GaAs power transistors [2]. For GaN HEMTs with 0.12 μm gates, devices with a current gain cut-off frequency f_τ of 121 GHz and power gain cut-off frequency f_{max} of 162 GHz have been reported [3]. A comparison of material properties relevant to high power, high frequency RF performance was given in Table 1.1.

This chapter begins by presenting small signal RF measurements of several devices. A small-signal device model is developed, and intrinsic and extrinsic elements that affect CAVET RF performance are identified. Studies are carried out to examine the effects of the gate-drain capacitance and the drain delay, and a complete time delay analysis is performed. Finally, DC characteristics of devices with varying gate overlap lengths L_{go} are measured in order to determine the minimum amount of gate overlap a device must possess in order to function properly.

6.2 RF device characterization

For our RF characterization, we chose to analyze Device A and Device C from Figure 5.12 in Chapter 5, which are shown again in Figure 6.1. We were inter-

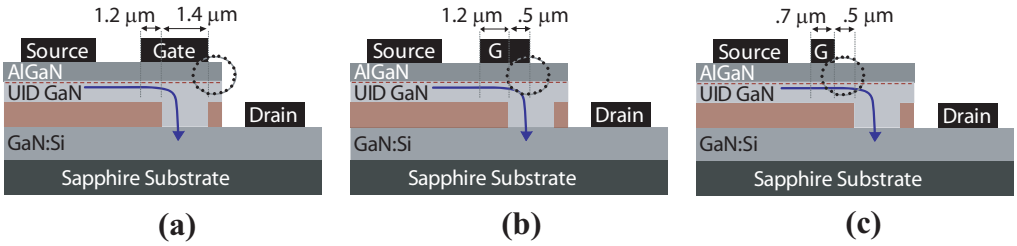

Figure 6.1: Ion implanted CAVETs analyzed for RF performance. (a) Device A. Gate completely covers the aperture. (b) Device B. Gate partially covers the aperture, drain-side edge of gate is near the current path. (c) Device C. Gate is completely offset from the aperture.

---

ested in these devices for the following reasons. Device A is a standard device, so the total delay measured in this device reflects all intrinsic and extrinsic parasitics present in a CAVET. Device C is very similar to a GaN HEMT, so we can determine whether this device performs as expected by comparing its RF performance to that of a HEMT with similar gate length.

Small-signal S-parameter measurements were performed using an Agilent Vector Network Analyzer. Plots of h_{21} and U for Device A and Device C from Figure 6.1 are illustrated in Figure 6.2. For both devices, h_{21} exhibited a roll off with frequency of approximately – 20 dB/decade, corresponding to a response from a single dominant pole. The current gain cut-off frequency f_τ was 5.6 GHz

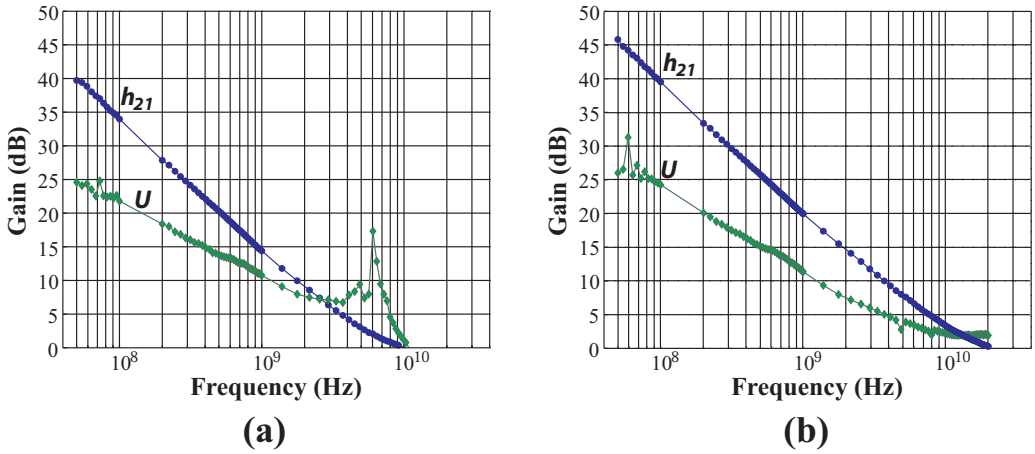

Figure 6.2: Small-signal short circuit current gain (h_{21}) and unilateral power gain (U) of (a) Device A and (b) Device C in Figure 6.1. The current gain cut-off frequency f_τ was 5.6 GHz for Device A and 12.3 GHz for Device C.

---

for Device A and 12.3 GHz for Device C.

The unilateral power gain U in these devices was extremely low and did not roll off at – 20 dB/decade. This suggests that U was dominated by the large extrinsic parasitics. It was therefore impossible to determine what effect the intrinsic parasitics may have had on f_{max}. To obtain power gain at high frequencies, it is necessary to first eliminate these extrinsic parasitics.

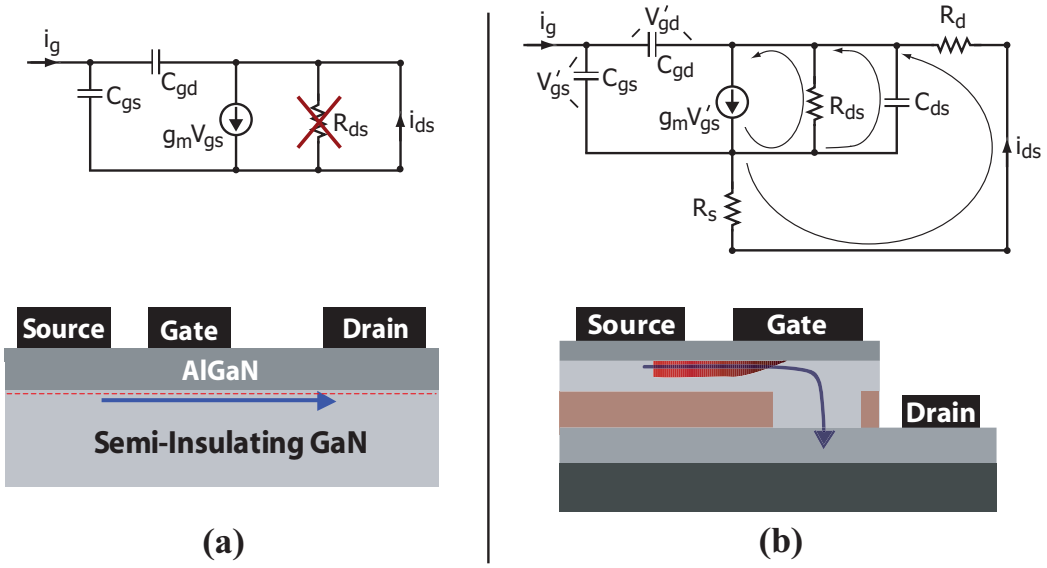

Figure 6.3: Small-signal model of (a) a HEMT and (b) a CAVET, indicating important terms for calculating f_τ.

6.3 Theoretical RF analysis

6.3.1 Small-signal device model

In order to analyze the RF performance of a transistor, it is necessary to first develop a small-signal analytic model. The small-signal model of a CAVET, along with the intrinsic model of a HEMT, are illustrated in Figure 6.3. For the

HEMT, the current gain cut-off frequency f_τ is given by:

$$f_\tau = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} = \frac{1}{2\pi\tau_t} \tag{6.3.1}$$

where g_m is the device transconductance and τ_t is the intrinsic or transit delay. For a GaN HEMT, the gate-drain capacitance C_{gd} is small and typically negligible compared to the gate-source capacitance C_{gs}. Since C_{gs} is proportional to L_g, f_τ is proportional to $(L_g)^{-1}$.

For a CAVET structure, predicting the RF characteristics is not nearly as straightforward as in a HEMT. Because the drain is located directly underneath the gate, C_{gd} may be large enough to have a significant impact on the RF performance. Also, in addition to the usual intrinsic parasitics which dominate the RF performance of a HEMT, a number of extrinsic parasitics exist in a CAVET which must be considerred in the RF analysis. These additional components are shown in the CAVET small signal model in Figure 6.3. The CAVET has an additional source-drain capacitance C_{ds} which is small and typically negligible in a HEMT. Also, in the CAVETs fabricated for this study, the source and drain access resistances, R_s and R_d, are relatively large and therefore cannot be ignored. At first inspection, it appears that impedences in series with the input and

output ports should only affect voltage, not current. However, Tasker *et al.* [4] have previously shown that the source-drain current is also effectively reduced. Since R_{ds} and C_{ds} are no longer shorted, the intrinsic source-drain current $g_m V_{gs}^{'}$ will divide between R_{ds}, C_{ds}, and the current path from source to drain, as indicated in Figure 6.3. Additionally, the voltage drop across C_{gd} is now larger than the drop across C_{gs} because of the IR voltage developed across R_s and R_d, which results in an effective increase in C_{gd} by a factor of $(1 + g_m{\cdot}R)$, where $R = (R_s + R_d)/(1 + (R_s + R_d)/Z_{ds})$ and Z_{ds} is the impedence of R_{ds} in parallel with C_{ds}.

6.3.2 Description of RF parameters

In order to optimize the CAVET for RF performance, it is important to identify the device dimensions and parameters that affect the RF characteristics. A number of device dimensions relevant to RF performance are illustrated in Figure 6.4. The parasitics which affect RF performance can be split into three categories: (1) intrinsic parasitics, (2) drain delay, and (3) extrinsic parasitics. Although the drain delay is considered an extrinsic parasitic, its effects will be treated sepa-

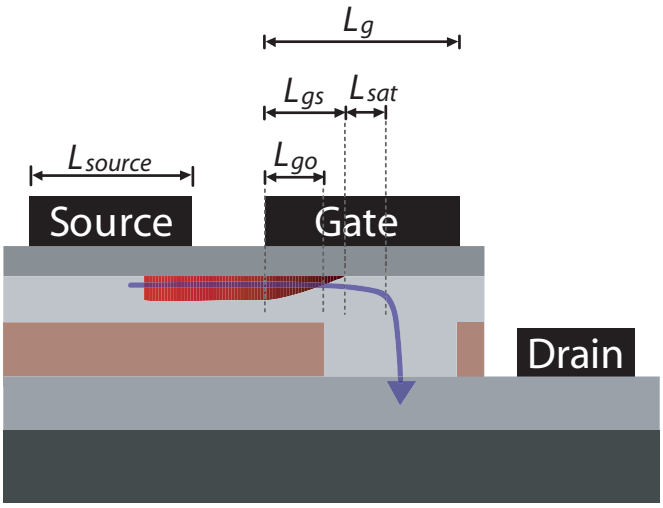

Figure 6.4: Schematic diagram of an AlGaN/GaN CAVET indicating various dimensions that are relevant to the device RF performance.

---

rately from the other extrinsic parasitics. The total delay τ_T in a CAVET can then be written as:

$$\tau_T = \tau_t + \tau_d + \tau_{ext} \tag{6.3.2}$$

where τ_t is the intrinsic or transit delay, τ_d is the drain delay, τ_{ext} is the extrinsic delay, and $\tau_T = 1/(2\pi f_\tau)$.

Intrinsic parasitics

The intrinsic delay τ_t in a CAVET is given by:

$$\tau_t = \frac{C_{gs} + C_{gd}}{g_m} \tag{6.3.3}$$

For a CAVET structure, predicting the values of C_{gs} and C_{gd} is not nearly as straightforward as in a HEMT. In a standard CAVET, such as Device A in Figure 6.1, the path of current flow does not pass under the entire gate. While the gate extends all the way to the end of the aperture, electrons begin moving downwards before reaching this point, as indicated in Figure 6.4. This means that only a portion of the intrinsic gate will contribute to C_{gs}. Also, because the aperture region is partially depleted by the implanted layer on either side, it is not obvious exactly how far electrons travel horizontally under the gate before reaching the saturation region. We therefore have defined L_{gs} as the distance electrons travel underneath the gate before the channel pinches off, and we have assumed L_{gs} to be slightly larger than L_{go}, as indicated in Figure 6.4. C_{gs} will therefore be proportional to L_{gs}.

Additionally, the gate-drain capacitance C_{gd} in the CAVET may be large enough to have a significant impact on the RF perfomance. This arises from the fact that

the gate lies directly above the drain, rather than off to the side of the drain. As a result, C_{gd} will be proportional to the total gate length L_g, which is shown in Figure 6.4. This is quite different from a HEMT, for which C_{gd} is relatively small and should not show a strong dependence on the gate length. It is therefore important to determine whether C_{gd} has a significant effect on the device RF performance.

Drain Delay

The drain delay τ_d must also be accounted for in the CAVET RF analysis. The drain delay was identified by Moll *et al.* [5] to be the delay associated with drift across the drain depletion region. In principle, for a CAVET, this would include drift in the horizontal depletion region under the gate as well as vertically through the aperture. However, since the CAVET was designed to have very little voltage drop vertically across the aperture, the overwhelming majority of τ_d will be associated with the horizontal velocity saturation region, which is labelled L_{sat} in Figure 6.4. In a standard HEMT, the lateral extent of the saturation region is small, resulting in a drain delay that is small compared to the total delay τ_T for devices in which the gate length is not too small. For the CAVET geometry,

the saturation region may be spread out over a larger distance, as was indicated in § 2.2, which results in a lower peak electric field than in a HEMT, but could also result in significant drift delays.

Extrinsic parasitics

Because of the vertical nature of the device, the source-drain capacitance C_{ds} of a CAVET is proportional to the length of the intrinsic source L_{source}, which is illustrated in Figure 6.4. C_{ds} can therfore be minimized by keeping L_{source} as small as possible. However, if L_{source} is made smaller than the contact transfer length, the source resistance may increase. In practice, source contacts can be designed such that C_{ds} is very close in value to C_{gd}. C_{ds}, as well as R_{ds}, will only affect f_τ if their impedences are comparable to $(R_d + R_s)$. Otherwise, τ_{ext} will be very small compared to τ_T.

Because the CAVET device process was not yet optimized for RF performance, extrinsic parasitics associated with the probing pads were also present in these devices. Prior to depositing the source and gate pads, the AlGaN underneath the pad area was etched away, and a layer of SiO_2 was deposited prior to deposition of the pads. This procedure effectively isolated the gate pad from the

source, reducing it to a remote fringing capacitance. However, due to the vertical nature of the device, this process did not isolate these pads from the drain region, so the extrinsic source-drain and gate-drain capacitances $C_{ds,ext}$ and $C_{gd,ext}$ were potentially large. While the effects on f_τ were expected to be small, both of these capacitances affect the unilateral power gain U.

With the implementation of an appropriate device process, it should be possible to eliminate extrinsic parasitics. In HBT technology, parasitics similar to those in the CAVET are inherently present. In AlGaAs/InGaAs HBT's, parasitics have been reduced by implementation of a transferred substrate Schottky collector process, and an f_{max} of 820 GHz has been demonstrated [6]. A similar process may be possible for GaN CAVETs.

6.4 RF performance: CAVET vs. HEMT

To determine whether our measured values of f_τ were approximately what one might expect, we compared the small-signal characteristics of Device C from Figure 6.1 to those of as standard HEMT. Schematics of these two devices are illustrated again in Figure 6.5. If extrinsic parasitics do not significantly affect

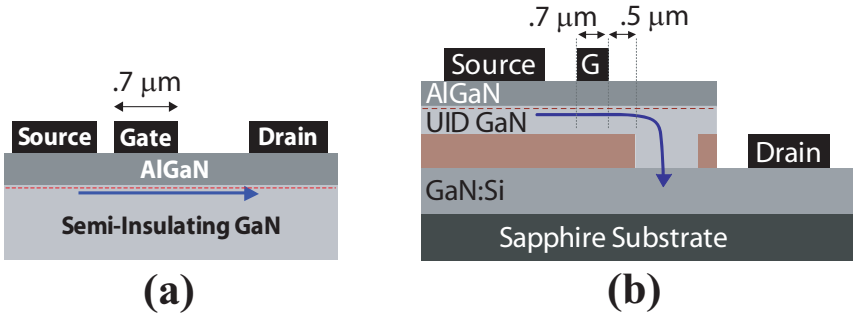

Figure 6.5: Devices compared for RF performance. (a) Standard GaN HEMT. (b) CAVET with an offset gate (Device C).

---

f_τ of Device C, then the current gain characteristics of this device should be identical to those of a GaN HEMT with a 0.7 μm gate. GaN HEMTs with gate dimensions and AlGaN layers that are identical to those of Device C typically have an f_τ of around 20 GHz [7], which is about 65% higher than that of the CAVET. However, the g_m of the HEMT is typically around 200 mS/mm, which is also about 65% higher than the g_m of the CAVET. Since f_τ is proportional to g_m, this would explain the disparity between the two devices. The g_m for the CAVET was probably low because of the lower charge and mobility in the 2DEG due to the regrowth process, as was detailed in § 5.5.3. This result gives an indication that extrinsic parasitics may not significantly affect τ_T.

6.5 Effects of C_{gd}

In a HEMT, C_{gd} is typically much smaller than C_{gs}, so its effects on the device RF performance are negligible. In a CAVET, because the drain is below the gate, it is conceivable that C_{gd} could be much closer in magnitude to C_{gs}. If this were the case, we would expect to see a reduction in f_τ. It is therefore important to determine whether C_{gd} has any impact on the device small signal performance.

In a CAVET, C_{gs} is primarily determined by the gate overlap length L_{go} (see Figure 6.4), so varying the aperture length L_{ap} while maintaining a constant value of L_{go} should not affect C_{gs}. However, C_{gd} is proportional to the total gate length L_g. Increasing L_{ap} while keeping L_{go} constant would cause an increase in L_g, so C_{gd} would also increase. Therefore, by measuring f_τ for devices with the same value of L_{go} but different values of L_{ap}, it is possible to ascertain whether or not C_{gd} has a measurable effect on the current gain of these devices.

In Figure 6.6, f_τ is plotted versus L_{ap} for five two-sided CAVETs which all had the same gate overlap length L_{go} but different aperture lengths L_{ap}. In these devices, $L_{go} = 1$ μm, and L_{ap} was varied from 1 μm to 2 μm. L_g was therefore 3 μm for the device with the smallest aperture and 4 μm for the device with

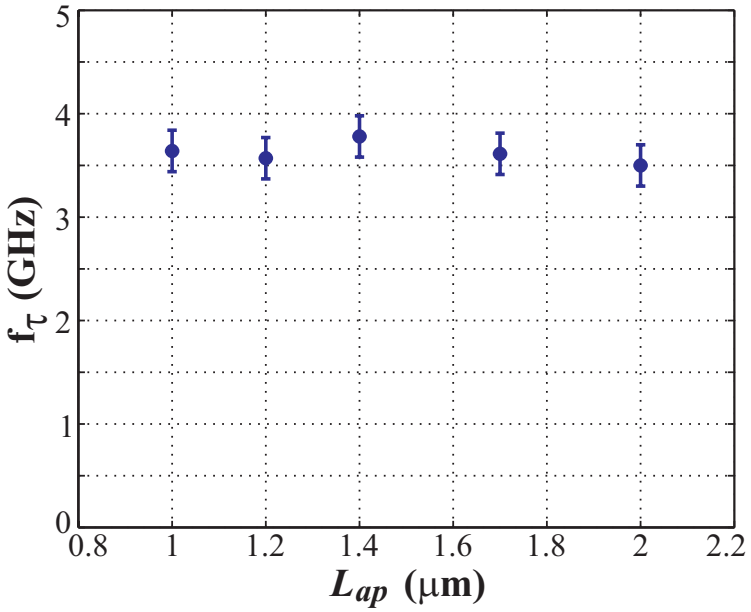

Figure 6.6: f_τ plotted versus L_{ap} for two-sided CAVETs which all had the same gate overlap length L_{go} but different aperture lengths L_{ap}. $L_{go} = 1$ μm for all five devices.

---

the largest aperture, corresponding to a 33% increase in C_{gd}. We can see that f_τ remained essentially constant for all the devices, indicating that C_{gd} is negligibly small as compared to C_{gs}. Additionally, a hand analysis of C_{gs} and C_{gd} predicts that C_{gs} is ~ 1 order of magnitude larger than C_{gd}.

S-parameter measurements of Device A and Device B in Figure 6.1 also confirmed the above conclusions. For these two devices, C_{gs} is the same, but C_{gd}

should belarger in Device A than in Device B. f_τ was measured to be 5.6 GHz in Device A and 5.7 GHz in Device B, indicating that C_{gd} was small and could be neglected.

6.6 Extrinsic Parasitics

The extrinsic parasitics shown in the small-signal device model in Figure 6.3 will only affect f_τ if either R_{ds} or $(2\pi f C_{ds})^{-1}$ is comparable in magnitude to $(R_d + R_s)$. If $(R_d + R_s)$ is much smaller than both of these impedences, than essentially all of the current $g_m V_{gs}$ will flow through i_{ds}, and so the effects of these parasitics will be negligible. Based on the comparison of a HEMT to Device C, which was detailed in §6.4, we would expect that these parasitics should not significantly affect f_τ. A hand analysis of these parasitics was conducted to determine whether they should affect f_τ.

From TLM measurements, $(R_d + R_s)$ was determined to be 2.0 $\pm$ 1.0 Ω·mm. From device I–V characteristics, R_{ds} was found to be larger than 120 Ω·mm for all devices, so R_{ds} was clearly much larger than $(R_d + R_s)$. To quantify the effects of C_{ds}, we again used Device C in Figure 6.1 as our reference. The

following analysis verified that in the frequency range of interest, $1/(2\pi f C_{ds})$ was significantly larger than $(R_d + R_s)$.

We first assume that $1/(2\pi f C_{ds})$ is significantly larger than $(R_d + R_s)$ for $f \leq f_\tau$ and verify this assumption at the end. Additionally, from a hand calculation, we found that $C_{ds} \approx 0.4 \cdot C_{gs}$, and g_m was taken to be 0.1 S/mm, which was the approximate measured DC value obtained in § 5.5.2. For Device C, since τ_d is expected to be negligible, if $1/(2\pi f_\tau C_{ds}) >> (R_d + R_s)$ and C_{gd} is negligible, then f_τ is given by the expression:

$$f_\tau = \frac{g_m}{2\pi C_{gs}} \tag{6.6.1}$$

This equation can be rearranged to read:

$$\frac{1}{g_m} = \frac{1}{2\pi f_\tau C_{gs}} = 10 \ \ \Omega \cdot \mathrm{mm} \tag{6.6.2}$$

Using the result in Eqn.6.6.2, we can obtain a value for $1/(2\pi f_\tau C_{ds})$:

$$\frac{1}{2\pi f_\tau C_{ds}} = \frac{1}{2\pi f_\tau (0.4 \cdot C_{gs})} = 25 \ \ \Omega \cdot \mathrm{mm} \approx 10 \cdot (R_d + R_s) \tag{6.6.3}$$

Because the impedence associated with C_{ds} is purely imaginary, the ratio $i_{ds}/g_m V_{gs}$ is given by:

$$\frac{i_{ds}}{g_m V_{gs}} = \left| \frac{1}{1 + j \cdot (0.1)} \right| \approx 0.995 \tag{6.6.4}$$

We can therefore see that C_{ds} does not have a significant impact on f_τ, and that our initial assumption that $1/(2\pi f C_{ds})$ is significantly larger than $(R_d + R_s)$ was correct. Our final conclusion is that the extrinsic parasitics in the CAVET do not have a significant impact on f_τ, or in other words $\tau_{ext} << \tau_T$.

6.7 Time delay analysis

Now that we have determined that the extrinsic parasitics in a CAVET do not significantly affect the total delay, we can divide the delay into two components: (1) the delay that occurs underneath the gate overlap region in Figure 6.4 and (2) the delay that occurs past L_{go} but prior to the point at which current begins to flow downwards, which is labeled point **a** in Figure 6.7. The second component of the delay results from the channel extending beyond the edge of the aperture, as illustrated in Figure 6.4, as well as from the drain delay. This second component of the total delay is of interest because it will be present in all standard devices where the gate metal extends above the aperture. The three devices in Figure 6.1 were used to calculate this delay.

Figure 6.7 helps illustrate how the delay associated with the region beyond

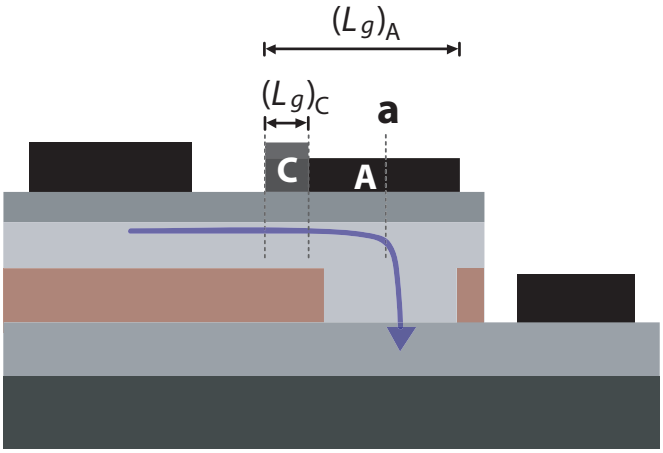

Figure 6.7: Illustration depicting how the delay above the aperture was determined. Point **a** indicates where current switches from horizontal to vertical flow. The two gates, labeled **A** and **C**, correspond to the gates of Devices A and C in Figure 6.1.

L_{go} was extracted, and the results are shown in Figure 6.8. For a device in which the gate is offset from the aperture, such as Device C, the total delay results from C_{gs}, so τ_T is proportional to the total gate length L_g. If the source-side edge of the gate is held fixed and the total gate length is increased (i.e. the drain-side edge of the gate is moved towards point **a**), the total delay will increase linearly with L_g until $L_g = L_{go}$. This is represented by the solid line passing through **c** in Figure 6.8. The total delay for a device with $L_g = L_{go}$ was extrapolated to be 22.4 psec, as indicated by the horizontal dashed line in Figure 6.8.

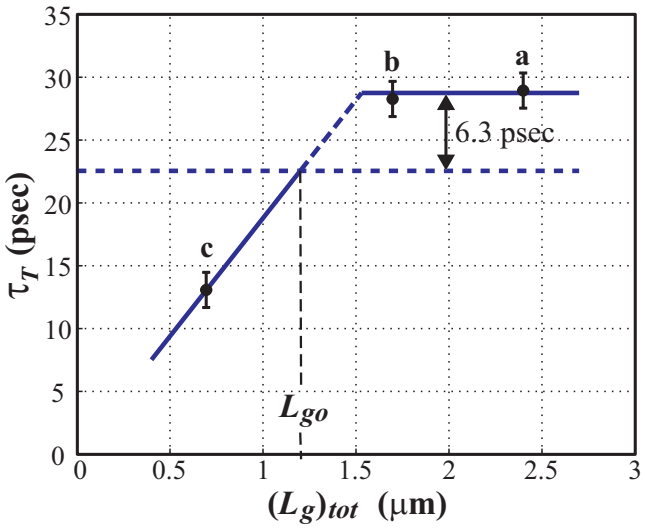

Figure 6.8: Plot of τ_T versus gate length L_g for the three devices in Figure 6.1, along with extrapolation of the delay associated with the region above the aperture.

As L_g is further increased, τ_T will continue to increase (although not necessarily at the same rate) until the drain side edge of the gate is at point **a**. If the total gate length is then further increased so that the gate extends beyond point **a**, τ_T will remain constant. The difference between τ_T for a device with $L_g = L_{go}$ and one in which L_g extends beyond point **a** is the delay which occurs between the edge of the aperture and point **a**. This delay was measured to be 6.6 psec.

As stated earlier, this delay of 6.6 psec results partially from the drain delay

and partly from the extension of the channel beyond the edge of the aperture region. However, it would be beneficial to know exactly how much of this delay is drain delay. In principle, it is possible to independently measure τ_d using a procedure described by Moll *et al.* [5]. However, attempts to perform these measurements on CAVET structures were unsuccessful due to both the significant amount of gate leakage in the devices as well as the rectifying nature of the source and drain contacts.

6.8 Optimization of L_{go}

In order to increase f_τ in a CAVET, it is necessary to decrease either τ_t or τ_d, or both. Decreasing τ_d could possibly be achieved by reducing the aperture length L_{ap}. However, any reduction in τ_d implies a possible reduction in the length of the horizontal depletion region L_{dep}, which would cause an increase in the peak electric field in the device. This would be extremely undesirable for large signal operation, since the breakdown voltage would be reduced. Reducing τ_t can be accomplished by reducing the gate overlap length L_{go}. It is therefore important to reduce L_{go} to as small a value as possible.

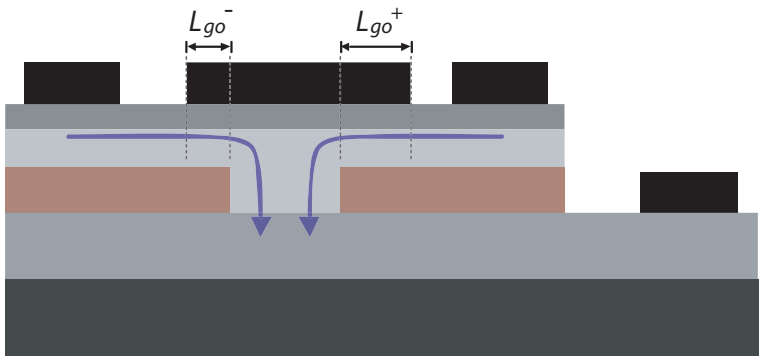

Figure 6.9: Due to the error inherent in the gate lithography, the center of the gate was offset from the center of the aperture by 0.2 μm. As a result, the gate overlap length was shorter on one side of the aperture (L_{go}^-) and longer on the other side (L_{go}^+).

In trying to reduce L_{go}, a number of considerations must be taken into account. First of all, if stepper lithography is used to define the gate, then the position of the gate will only be accurate to within about 0.2 μm, so this error must be accounted for. Second, if L_{go} is made extremely small, then current will enter the aperture without being modulated by the gate, in which case normal DC device operation cannot occur. Finally, if L_{go} is large enough for devices to operate normally under small DC biases, but it is still very small, then source leakage underneath the 2DEG could possibly become a problem at larger biases.

In order to determine how small L_{go} could be made without affecting DC

device performance, two-sided CAVETs with different values of L_{go} were fabricated, and DC I–V characteristics were obtained. The error in the position of the gate relative to the aperture was measured to be 0.2 μm, which meant that for each device, L_{go} differed by 0.4 μm from one side of the device to the other, as illustrated in Figure 6.9. Therefore, for each measurement that was performed, only one source was contacted, and the value of L_{go} that was reported corresponded to the side of the device that was measured.

The DC I–V curves of four CAVETs with varying gate overlap lengths are shown in Figure 6.10. The devices all had an aperture length $L_{ap} = 1.4$ μm, and the gate overlap lengths L_{go} were – 0.2 μm (i.e. gate was smaller than the aperture), 0.1 μm, 0.2 μm, and 0.5 μm The leakage currents observed in devices (b)–(d) were shown to result entirely from gate leakage. For the device in which the gate does not completely cover the aperture region, it is clear that most of the current is not modulated by the gate, so normal DC device operation cannot be achieved. For the other three devices, even when L_{go} was as small as 0.1 μm, ideal DC behavior was observed for relatively low source-drain voltages, suggesting the possibility of CAVETs which could operate at very high frequencies. However, because of the gate leakage in these devices, it was impossible

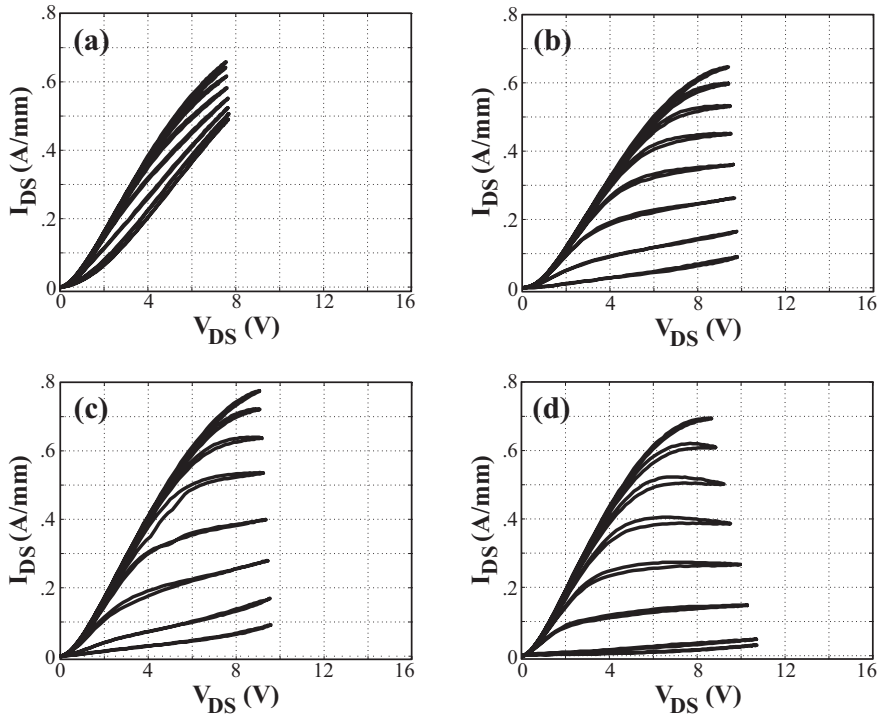

Figure 6.10: DC I–V curves of CAVETs with varying L_{go}. For these devices, $L_{ap} = 1.4$ μm and L_{go} was (a) – 0.2 μm, (b) 0.1 μm, (c) 0.2 μm, and (d) 0.5 μm. Leakage currents in devices (b)–(d) were completely due to gate leakage.

---

to determine whether the large-signal characteristics of devices with such small gate overlap lengths would suffer from source leakage underneath the 2DEG.

The results in this section suggest that an appropriate gate overlap length for a CAVET designed to operate at high frequencies is approximately 0.3–0.4 μm. It is necessary to maintain an overlap of at least 0.1–0.2 μm in order to obtain ideal

DC operation, and an error of $\sim$ 0.2 μm in the lithography must be accounted for, which leads us to this suggested value. For a device with $L_{go} = 0.3$ μm, the predicted value of τ_T is given by:

$$\tau_T = 5.5\text{ps} + 6.3\text{ps} = 11.8\text{ps} \tag{6.8.1}$$

corresponding to an f_τ of $\sim$ 13.5 GHz. We can see from Eqn.6.8.1 that the delay occurring beyond the edge of the aperture region (6.3 psec) accounts for over half of the total delay.

6.9 Summary

An RF analysis of AlGaN/GaN CAVETs with implanted insulating layers was performed, and current gain cutoff frequencies as high as 12.3 GHz were demonstrated. A small signal device model was developed, and a time delay analysis was performed to determine which elements in the device model significantly contributed to the total delay τ_T in the device. Experimental results indicated that C_{gd} did not significantly contribute to τ_T. In addition to the intrinsic delay associated with the gate-overlap, a delay τ_{ext} of 6.3 psec was measured for devices for which the gate extends a significant distance beyond the source-side

edge of the aperture. This delay was attributed to two seperate effects: (1) the channel extending beyond the edge of the aperture before pinching off, and (2) the drain depletion region being smeared out over a significantly large distance, resulting in a non-negligible drain delay. Finally, based on DC measurements of devices with varying values of L_{go}, a minimum gate overlap of 0.1–0.2 μm was found to be a requirement for ideal DC performance. If stepper lithography is to be used to define the gate, then L_{go} should be set to at least 0.3–0.4 μm, since an error of $\sim$ 0.2 μm in the lithography must be accounted for.

References

[1] Cree achieves major advance in gallium nitride transistor power density. Press release, Durham, NC, December 15, 2003.

[2] K. Asano, Y. Miyoshi, K. Ishikura, Y. Nashimoto, M. Kuzuhara, and M. Mizuta. Novel high power AlGaAs/GaAs HFET with a field-modulating plate operated at 35 V drain voltage. *International Electron Devices Meeting 1998 Technical Digest*, 59–62, 1998.

[3] V. Kumar, W. Lu, R. Schwindt, A. Kuliev, G. Simin, J. Yang, M. A. Khan, and I. Adesida. AlGaN/GaN HEMTs on SiC with f_T of over 120 GHz. *IEEE Electron Device Letters*, 23(8):455–7, 2002.

[4] P. J. Tasker and B. Hughes. Importance of Source and Drain Resistance to the Maximum f_T of Millimeter-Wave MODFET's. *IEEE Electron Device Letters*, 10(7):291–3, 1989.

[5] N. Moll, M. R. Hueschen, and A. Fischer-Colbrie. Pulse-Doped AlGaAs/InGaAs Pseudomorphic MODFET's. *IEEE Transactions on Electron Devices*, 35(7):879–86, 1988.

[6] M. Rodwell, Q. Lee, D. Mensa, J. Guthrie, Y. Betser, S. C. Martin, R. P. Smith, S. Jaganathan, T. Mathew, P. Krishnan, C. Serhan, and S. Long. Transferred-substrate heterojunction bipolar transistor integrated circuit technology. *Conference Proceedings, Eleventh International Conference on Indium Phosphide and Related Materials*, 169–74, 1999.

[7] Robert Coffie. *Characterizing and Suppressing DC-to-RF Dispersion in AlGaN/GaN High Electron Mobility Transistors*. PhD thesis, University of California, Santa Barbara, 2003.

7

Summary, conclusions, and future work for the AlGaN/GaN CAVET

7.1 Summary and conclusions

THIS dissertation has focused on the development of the AlGaN/GaN current aperture vertical electron transistor. Since this device was the first of its kind, much of the effort was spent on developing a model which accurately predicted device performance, development of growth and processing techniques, and device DC charaterization. In addition, leakage currents and DC-RF dispersion were fully investigated, and a detailed RF analysis was conducted. In all, three generations of devices were fabricated, each showing significant improvements in performance over previous ones.

The first CAVETs fabricated contained regrown aperture and source regions,

and the insulating layers were doped with either iron or magnesium. These devices had very low current densities, which was shown to result from iron or magnesium being incorporated into the regrown material. Additionally, the insulating properties of the Fe-doped layer were found to be insufficient to prevent significant source-drain leakage.

For the second generation of CAVETs, devices with Mg-doped insulating layers were fabricated, and improved processing techniques insured that the magnesium rich surface layer was removed prior to regrowth, thus preventing magnesium from incorporating into the regrown material. The result was devices with maximum source-drain currents I_{max} as high as 750 mA/mm, which is slightly lower than that of state-of-the-art GaN HEMTs but still comparable. Additionally, these devices exhibited almost no DC-RF dispersion. The analysis of dispersion performed in Chapter 3 showed conclusively that the dispersion prevalent in GaN HEMTs is indeed surface related, and since there is no surface on the drain side of the gate in the CAVET geometry, DC-RF dispersion is mitigated. The most prominent issue with these devices was large leakage currents, which were evident in all the I–V curves.

Leakage currents were fully characterized in Chapter 4 and were found to

be comprised of three elements: (1) electrons from the source passing directly through the insulating layer, (2) electrons from the source traveling through the aperture but underneath the 2DEG so that they are not modulated by the gate, and (3) electrons traveling from the gate to the drain. Source leakage was successfully eliminated by optimizing regrowth conditions and device design. However, gate leakage still remained a problem. Gate leakage was found to result from the high unintentional n-type doping of material inside and above the aperture region, which was grown on a vertical or inclined plane, as opposed to in the c-direction. It is necessary to be able to control the doping levels of the material inside and above the aperture region in order to eliminate gate leakage as well as to increase the breakdown voltage.

The third generation of CAVETs took advantage of an aluminum ion implantation to define the insulating layer. This process allowed for a completely planar regrowth, thus allowing doping levels inside and above the aperture region to be precisely controlled. Resulting devices exhibited record high current densities (780 mA/mm) with greatly reduced leakage and very little DC-RF dispersion. However, gate leakage was not completely eliminated and led to relatively low breakdown voltages. Studies indicated that leakage was still related to the ma-

terial directly above the aperture, which possibly was unintentionally doped by contaminants from the implant mask that could not be fully removed prior to regrowth. It is probably necessary to employ an insulator underneath the gate metal to reduce gate leakage to acceptable levels and achieve higher breakdown voltages.

Small signal RF characteristics were measured for third generation CAVETs, and current gain cutoff frequencies f_τ as high as 12.3 GHz were demonstrated. The gate overlap length L_{go} was found to be the dominant factor in determining the intrinsic delay, while the additional delay that was measured was attributed to a combination of drain delay as well as extension of the horizontal channel region beyond the edge of the aperture before it pinched off. With respect to the current gain, the effects of C_{gd}, C_{gs}, and the source and drain access resistances R_d and R_s appeared to be minimal. However, the power gain U was dominated by large extrinsic parasitics, which must first be eliminated before RF power performance can be achieved.

7.2 Future work

Initially, further work on the CAVET should focus on three areas: (1) reducing gate leakage and increasing breakdown, (2) improving RF performance, and (3) simplifying the device process. Even for devices with implanted insulating layers, gate leakage was still an issue. As was suggested in Chapter 5, this problem could probably be corrected by deposition of a 25 Å SiN layer for a gate insulator while the wafer is inside the MOCVD reactor for the regrowth step. This process has been shown to work in GaN MESFETs [1], and power densities as high as 6 W/mm have been achieved.

In order to achieve RF power performance, it is necessary to eliminate the large extrinsic parasitics that were present in the devices fabricated for this work. Unfortunately, this further complicates the process even more. Probably the best approach to achieving this goal is to utilize a flip-chip bond and transferred substrate process, as is used in HBT technology [2].

Finally, one of the major dissadvantages of CAVET technology in its current status is that the device fabrication is excessively complicated. For the third generation of CAVETs, the entire process involved ten lithography steps, three

material growth steps (initial growth plus two regrowths), and an ion implantation. Additionally, accurate alignment was critical in four of the lithography steps. If a flip-chip process was to be implemented, this would add several additional steps as well. For comparison, the standard UCSB HEMT process only involves a single growth and four lithography steps, and careful alignment is only critical in one of the lithography steps. In order to improve reliability and reproducibility of CAVETs, it is critical to simplify this process.

Looking further ahead, if wafer fusion is developed as a viable option for semiconductor electronic device technology, the CAVET would be a prime candidate for a device that takes advantage of multiple material systems. For example, a CAVET consisting of an AlGaAs/GaAs heterostructure fused to GaN could potentially benefit from the high 2DEG mobilities that are possible in the GaAs system while still taking advantage of the high breakdown field and large thermal conductivity in GaN.

References

[1] A. Chini, D. Buttari, S. Keller, and U. K. Mishra. to be published.

[2] M. Rodwell, Q. Lee, D. Mensa, J. Guthrie, Y. Betser, S. C. Martin, R. P. Smith, S. Jaganathan, T. Mathew, P. Krishnan, C. Serhan, and S. Long. Transferred-substrate heterojunction bipolar transistor integrated circuit technology. *Con-*

ference Proceedings, Eleventh International Conference on Indium Phosphide and Related Materials, 169–74, 1999.

A

Specifics of MOCVD regrowth

ALTHOUGH growth conditions for the CAVET base structure were given in Chapter 2, details of the regrowth conditions were not presented earlier, so they are covered in this section. Conditions for the regrowth of the aperture and source region as well as that of the ohmic contact region are described here.

For the aperture and source regrowth, the etched wafer was inserted into the

MOCVD reactor, and the reactor temperature was ramped from room temperature to 1050 °C in 180 seconds at a pressure of 300 torr. During this ramp step, 3 slpm of NH_3 and 9 slpm of N_2 were injected into the reactor. Once the temperature reached 1050 °C, a small amount of TMGa (10 sccm) was injected into the reactor, and at the same time the temperature was ramped from 1050 °C to 1160 °C in 60 seconds. By the time the temperature reached 1160 °C, interrupted growth studies showed that the aperture region had partially filled with GaN. After the temperature reached 1160 °C, approximately 200 Å of GaN were grown at 300 torr in 3 slpm of NH_3, 9 slpm of N_2, and 10 sccm of TMGa. The slow growth rate ($\sim$ 0.2 μm/hr) was maintained in order to give the surface time to planarize. After this, the remaining 1500–2800 Å of UID GaN was grown at 760 torr in 6 slpm of NH_3, 6 slpm of N_2, and 60 sccm of TMGa, corresponding to a growth rate of $\sim$ 2 μm/hr. The AlGaN cap was grown in 3 slpm of NH_3 and 9 slpm of N_2 at 1140 °C and 100 torr, and the growth rate was $\sim$ 0.25 μm/hr. Table A.1 lists the exact growth conditions for each step of the regrowth.

For the ohmic contact regrowth, which was described in § 5.2.3, the patterned wafer was reinserted into the MOCVD reactor, the temperature was ramped to 1160 °C in 180 seconds in 7 slpm of NH_3 and 5 slpm of H_2, and a pressure of 760

Layer	Thick [Å]	Time [s]	Temp [°C]	Press [Torr]	NH_3 [slpm]	N_2 [slpm]	TM(Ga/Al) [sccm]
Temp 1	N/A	180	20→1050	300	3	9	N/A
Temp 2	N/A	60	1050→1160	300	3	9	10/0
GaN 1	200	300	1160	300	3	9	10/0
GaN 2	2800	470	1160	760	6	6	60/0
AlGaN	250	330	1140	100	3	9	7/12

Table A.1: Regrowth conditions for CAVET aperture and source regions.

torr was maintained. Once the temperature reached 1160 °C, 6 sccm of TMGa was injected into the reactor in addition to the NH_3 and H_2. This step lasted 2 minutes, after which the sample was cooled in NH_3 and N_2 and removed from the reactor.